High-Frequency Bandpass Delta-Sigma Analog-to-Digital Conversion

by

Frank W. Singor

A thesis submitted in conformity with the requirements for the Degree of Master of Applied Science
Department of Electrical Engineering
University of Toronto

© Copyright by Frank Wayne Singor 1994
High-Frequency Bandpass Delta-Sigma Analog-to-Digital Conversion

Frank W. Singor
Department of Electrical Engineering
University of Toronto,
Degree of Master of Applied Science, 1994

Abstract

This thesis demonstrates that analog-to-digital (A/D) conversion at the intermediate-frequency stage of a radio is feasible for a wide range of cellular and cordless telephony standards. Placing the A/D converter as close as possible to the front end of the radio has manufacturing advantages and allows the use of sophisticated DSP algorithms which are especially useful with digitally coded transmissions. The type of conversion proposed is a switched-capacitor (switched-C) implementation of a bandpass delta-sigma (BPΔΣ) modulator. This thesis addresses the performance of BPΔΣ A/D converters by focusing on larger bandwidths (1.2MHz) and higher centre frequencies (20MHz) than previously obtained, while maintaining 12 bit resolution.

An 8th-order 3-level BPΔΣ A/D modulator is designed to meet these specifications. Through modelling and simulation, it is shown that for low oversampling ratios large gains in signal-to-noise ratio cannot be obtained when going to higher-order modulators. However, by increasing the number of levels in the quantizer, the performance of the modulator can be greatly enhanced by taking advantage of the added stability.

Two 2nd-order BPΔΣ A/D modulator prototypes were implemented in a 0.8μm BiCMOS process to determine the maximum sampling frequency obtainable in a switched-C technology. The two structures both use fully differential OTAs with continuous-time common-mode feedback, but employ different clock phasing to experiment with trade-offs between active and passive sensitivities. An analysis of the effects of non-ideal OTAs on the switched-C biquads is done and compared to experimental results with very good correlation.
Acknowledgments

A special thanks to my supervisor Martin Snelgrove for introducing me to the wonderful world of bandpass delta-sigma modulation. His interest in this work and connections have kept things running smoothly, from getting silicon for me on BNRs test run, to providing research associates to test the fabricated parts. Thanks boss.

A big thanks also goes to Steve Jantzi whose help and guidance from the beginning of this work to the end has been a constant encouragement. Thanks for taking on the role of a “co-supervisor”.

Ralph “editor” Duncan also deserves recognition for pushing me to get my --- in gear and write this thesis up. Thanks for the hours you’ve spent proof reading and the valuable words ‘Write it up! You’re the only one who will ever read it’.

Thanks to Theodore Varelas for putting in the extra hours when I was in a rush to get a clock generator and when we needed test results. Many others would have described locations that I could have gone to instead.

There are many others that have helped in the course of this research but to properly thank them all, this section could become longer than the thesis itself. So to just name a few (reverse alpha): Sorin Voinigescu, Kumar Venguswamy, Brian Silveira, Ayal Shoval, Mark Schumacher, Richard Schreier, Bryn Owen, Chris Ouslis, Luc Lussier and Duncan Elliott.

For financial support, without which I would have been a very skinny man, thanks goes to the Natural Science and Engineering Research Council of Canada and Micronet.

Finally, and quite possibly most important, thanks to Cynthia Barnes for putting up with all those Friday night dates sitting in the lab watching me type away at this terminal. Thanks Cynth.
Table of Contents

Abstract........................................................................................................... ii
Acknowledgments............................................................................................. iii
Table of Contents............................................................................................. iv
Glossary of Terms............................................................................................. vii

CHAPTER 1

Introduction....................................................................................................... 1
1.1 Digital Radio................................................................................................. 1
1.2 Specification to Guide Design....................................................................... 2
1.3 Thesis Outline............................................................................................... 4

CHAPTER 2

Background........................................................................................................ 5
2.1 ΔΣ A/D Conversion.................................................................................... 5
  2.1.1 Modulation............................................................................................. 6
    2.1.1.1 Quantization Noise and Oversampling........................................ 7
    2.1.1.2 Positioning the Band................................................................. 8
    2.1.1.3 Modulator Order....................................................................... 10
  2.1.2 Decimation............................................................................................ 11
    2.1.2.1 Lowpass Decimation............................................................... 11
    2.1.2.2 Bandpass Decimation............................................................ 11
  2.2 Implementation of ΔΣ modulators............................................................ 12
    2.2.1 Topologies....................................................................................... 12
  2.3 Summary................................................................................................... 13
CHAPTER 3

Multi-Level ΔΣ A/D Converters .................................................. 15
3.1 High Gain Noise Transfer Functions ........................................ 15
3.2 BPΔΣ Modulators with High Gain NTFs ................................. 16
3.3 Linearity Problems with the D/A Converter ............................ 19
   3.3.1 Randomizing the levels in the D/A Converter ..................... 20
3.4 3-level 8th-Order BPΔΣ Modulator ....................................... 21
   3.4.1 3-level Decimation .................................................... 22
3.5 Summary .............................................................................. 23

CHAPTER 4

High-Speed Circuits .................................................................. 24
4.1 Operational Amplifier Design ................................................. 24
4.2 Comparator .......................................................................... 29
4.3 Switches .............................................................................. 29
4.4 Clock Generation .................................................................. 32
4.5 D/A Converter ...................................................................... 32
4.6 Sample-and-Hold .................................................................. 34
4.7 Summary .............................................................................. 34

CHAPTER 5

2nd-Order Bandpass ΔΣ Modulator Prototypes ............................. 36
5.1 Designing the Prototypes ....................................................... 36
   5.1.1 LDI Modulator .............................................................. 38
      5.1.1.1 OTA Loading in the LDI structure ......................... 40
   5.1.2 FE Modulator ............................................................... 42
      5.1.2.1 OTA Loading in the FE structure ......................... 43
   5.1.3 Scaling Capacitors ......................................................... 44
   5.1.4 Capacitor Mismatches ................................................... 45
   5.1.5 Non-ideal OTAs ........................................................... 46
5.2 Layout and Experimental Results .......................................... 51
   5.2.1 Folded Cascode OTA .................................................... 51
5.2.2 2nd-order Bandpass ΔΣ modulators ......................................................... 53
5.3 Summary ........................................................................................................ 56

CHAPTER 6

Conclusions and Future Work ................................................................. 57
6.1 Thesis Conclusions ................................................................................... 57
6.2 Future Work ............................................................................................... 59

APPENDIX A

Effects of Non-ideal OTAs on Switched-C Biquads ................................. 64
A.1 1/2-Delay Non-inverting Integrator ......................................................... 64
  A.1.1 OTAs with Finite DC Gain ................................................................. 65
  A.1.2 OTAs with Finite Bandwidth and Slew Rate Limitations .................. 66
A.2 1-Delay Non-inverting Integrator ............................................................ 70
  A.2.1 OTAs with Finite DC Gain ................................................................. 71
  A.2.2 OTAs with Finite Bandwidth and Slew Rate Limitations .................. 72
A.3 Errors expected with the LDI Biquad ...................................................... 74
A.4 Errors expected with the FE Biquad ......................................................... 76

References ...................................................................................................... 79
A/D .......... analog-to-digital
A(z) .......... loop-filter response
β ................ feedback factor
BNR .......... Bell-Northern Research
BPAΣ .......... bandpass delta-sigma
BW .......... bandwidth
ΔΣ .......... delta-sigma
D/A .......... digital-to-analog
DSP .......... digital signal processing
FE .......... forward Euler
FIR .......... finite impulse response
f_b .......... bandwidth
f_o .......... centre frequency
f_s .......... sampling frequency
IF .............. intermediate frequency
KCL .......... Kirchhoffs current law
LDI .......... lossless discrete integrator
LPΔΣ .......... lowpass delta-sigma
LPF .......... lowpass filter
MASH .......... multi-stage noise shaping
N ............. order of modulator
NTF (H_q) ...... noise transfer function
op-amp ........ operational amplifier
OSR .......... oversampling ratio
OTA .......... operational transconductance amplifier
SNR .......... signal-to-noise ratio
S/H .......... sample-and-hold
SR .......... slew rate
STF .......... signal transfer function
U (u) .......... input signal
RF .......... radio frequency
RFU .......... radio frequency unit
ROM .......... read-only-memory
VLSI .......... very large scale integration
CHAPTER 1

Introduction

This thesis deals with improving the performance of bandpass delta-sigma (BΔΣ) A/D modulators in two areas: larger relative bandwidths and higher sampling frequencies. Modelling and simulation work is used to explore architectures for the low oversampling ratios needed, while experimental work verifies the practicability of the high-speed switched-capacitor circuits needed.

Several BΔΣ modulators have previously been developed [1][2][3], but their centre frequencies were too low to make the bandpass approach to A/D conversion attractive to the digital radio market.

This thesis contributes to knowledge of architectural trade-offs in delta-sigma modulation, to high-speed BiCMOS analog circuit design, and to radio architecture.

1.1 Digital Radio

Moving signal processing in a radio to the digital domain is very attractive since it can result in a high performance radio that is small in size, low in cost and requires a minimal amount of initial calibration and on-going maintenance. The robustness of the digital circuitry not only gives manufacturing advantages but it also allows the use of sophisticated DSP algorithms, which are especially useful with digitally coded transmissions.

Ideally, it would be nice if the A/D converter could be connected directly to the antenna, thus eliminating the need for any analog mixing stage, but we are still a few years from a process which is capable of operating at these speeds. However, there is industrial interest in A/D conversion at the intermediate-frequency (IF) stage of a radio in-band [4], since this would still allow IF filtering, frequency selection and demodulation to be done
digitally. A/D conversion could also be done in quadrature at baseband, using a “zero-IF” receiver, but that requires precision matching and is susceptible to a variety of DC instabilities and electromagnetic compatibility problems. A comparison of both systems is shown in Fig. 1.1. Although ΔΣ techniques are shown for performing the A/D conversion, any suitable A/D conversion technique could be used.

![Digital Radio Architectures Diagram](image)

**FIGURE 1.1** Possible digital radio architectures

a) Direct-conversion using lowpass ΔΣ ND conversion.

b) Digital quadrature-IF using bandpass ΔΣ A/D conversion.

### 1.2 Specification to Guide Design

Challenging specifications to help set the course of this work were obtained from a Communications Research Centre (CRC) report [4]. This report outlined a possible future for the implementation of a proof-of-concept fully digital mobile radio. This system would employ several different radio frequency units (RFU) each tuned to a different frequency band. There would be an RF band select which would connect the desired RFU and mix
the signal down to some high IF on which A/D conversion would take place. The signal would then be mixed down to baseband where frequency selection, filtering and demodulation could all be done digitally. This would reduce size and cost while increasing yield.

![RF Channel Select Diagram]

**FIGURE 1.2** Possible architecture for a Future Mobile Digital Radio

The original system assumed a broadband 8 bit 5ash A/D converter running at 28OMHz giving roughly 9 bit accuracy in a 4OMHz band (or 12 bits in 1MHz) through oversampling. However, since the interest is only in an accurate representation of a small band of frequencies around some high IF it would be a perfect situation to use a **BPΔΣ** A/D converter. Specifications required from a **BPΔΣ** A/D converter are given in Table 1.1.
TABLE 1.1 Digital radio specifications for BPAΣ A/D converter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling frequency</td>
<td>80MHz</td>
</tr>
<tr>
<td>Centre frequency</td>
<td>20MHz</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>1.2MHz</td>
</tr>
<tr>
<td>Resolution</td>
<td>12 bits</td>
</tr>
<tr>
<td>Power</td>
<td>&lt;100mW</td>
</tr>
</tbody>
</table>

1.3 Thesis Outline

Improving the performance of the BPAΣ modulator is the main focus of this thesis. The two main objectives that will be addressed are increasing the centre frequency and bandwidth of the BPAΣ modulator.

Chapter 2 begins with a brief history of BPAΣ converters. An explanation of how ΔΣ A/D converters work is also given with a comparison between lowpass and bandpass ΔΣ modulators. Chapter 3 investigates the use of high gain noise transfer functions and multi-level quantizers as a way of obtaining high accuracy BPAΣ A/D modulators, in spite of low oversampling ratios. Chapter 4 goes through the design of the fully differential circuits required to implement the modulator. Chapter 5 contains the design, implementation and test results of two different type of 2\textsuperscript{nd}-order BPAΣ modulators which were designed to determine the upper sampling frequency obtainable in the switched-C technology. Chapter 6 contains the thesis conclusions and future work section, which gives the design of an 8\textsuperscript{th}-order 5-level BPAΣ A/D modulator. An appendix is also given which contains the calculations for the effects of non-ideal OTAs on the performance of switched-C biquads.
CHAPTER 2

Background

Representing an analog signal by a single bit, high speed bit stream has been of interest ever since delta modulation was first introduced in 1946. Delta modulation suffered from many problems which were later overcome in 1963 by delta-sigma (AZ) modulation [5]. ΔΣ modulation did not gain much popularity in the early days because of the expensive digital signal processing (DSP) that was required on the high-speed bit stream. Today, however, with fine line VLSI processes, the DSP which is required is very robust and affordable. Many “lowpass” ΔΣ (LPΔΣ) A/D converters have since been implemented and are commercially available. Recently, a new “twist” has been added to the standard LPΔΣ A/D converter [6][7][8]. Instead of making an accurate representation of the baseband signals, an accurate representation of a passband centered at some non-DC frequency is made. This approach is termed bandpass AZ (BPΔΣ) A/D conversion. In 1992 the first totally monolithic BPΔΣ A/D converter was implemented and the concept proven [1].

In this chapter the operation of the ΔΣ A/D converter is reviewed. The difference between lowpass and bandpass ΔΣ A/D converters will be discussed and a comparison in converter order versus signal-to-noise ratio (SNR) shown. Different methods of implementing the ΔΣ modulator will also be investigated.

2.1 ΔΣ A/D Conversion

ΔΣ A/D converters consist of two main sections: the modulator and the decimator. The modulator takes an analog input and represents it by a high-speed low-resolution stream of words. The decimator takes this high-speed bit stream and slows it down to the
Nyquist rate while increasing the length of the word such that no signal information is lost [9].

2.1.1 Modulation

To analyze the ΔΣ modulator, the A/D and D/A converters are replaced by additive white noise sources’ (Fig. 2.2). With the two white noise sources in place the methods of linear circuit analysis can be used to obtain an expression for the output $Y(z)$:

$$Y(z) = \frac{D(z)A(z)}{1 + A(z)} U(z) + \frac{1}{1 + A(z)} N_q(z) + \frac{A(z)}{1 + A(z)} N_d(z)$$

(2.1)

The quantization error (noise) made by the low resolution A/D converter sees a transfer function to the output of: $H_q(z) = 1/(1 + A(z))$, which we refer to as the “noise transfer function” (NTF). Thus, by properly selecting the poles of the filter ($A(z)$) one can effec-

---

1. Methods for converting non-linearity in the D/A converter into white noise have been developed [24] and will be discussed in chapter 3.
tively reduce the amount of quantization noise in the output (Y(z)) in a certain band of
frequencies. The noise injected by the low resolution D/A converter is not as fortunate.
Any error generated here sees a transfer function to the output of approximately 1 (in the
band of interest). Therefore, the low resolution D/A converter needs to be accurate to the
overall resolution of the complete ΔΣ A/D converter. The signal (U(z)) sees a transfer
function to the output given by: \( H_u(z) = \frac{D(z)A(z)}{1 + A(z)} \). The filter D(z) can be simplified if
poles of the signal transfer function (STF) are chosen to be the same as the poles seen by
the quantization noise. This would result in filter D(z) being very simple to implement
with just a few extra feed-in capacitors.

2.1.1.1 Quantization Noise and Oversampling

The rms value of the quantization error, assuming it is white and has an equal proba-
bility of lying anywhere in the range \( \pm \Delta/2 \), where \( \Delta \) is the level spacings in the A/D, is
given by (eq. 2.2).

\[
e_{\text{rms}} = \sqrt{\frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e^2 \text{d}e} = \frac{\Delta}{\sqrt{12}}
\]  
(2.2)

When the signal is sampled at \( f_s \) all of this quantization noise folds into a frequency band
\( 0 \leq f \leq f_s / 2 \) and has a total noise power of \( \Delta^2 / 12 \). As an example, the total noise power
for a 2-level quantizer (±1 V) is -4.77dB relative to \( 1V_{\text{rms}} \); increasing the number of
quantization levels to 3 (1 V, O V, -1 V) results in decreasing the total noise power by
3.5dB. Another way of decreasing the noise power in-band, without increasing the number
of quantization levels, is to sample at a frequency higher than the Nyquist rate. The spec-
tral density of the white quantization noise is \( E(f) = e_{\text{rms}}/\sqrt{f_s/2} \). The amount of noise
power \( (N_0^2) \) in the band of interest \( (0 \rightarrow f_b) \) can be determined using (eq. 2.3).
From this result it is easy to see that every doubling of the oversampling ratio (OSR) will decrease the in-band noise power by 3dB. This effect can be enhanced by using ΔΣ modulation techniques which have the ability to shape the quantization noise, pushing it out of the band of interest. This is illustrated in (eq. 2.4) where it is seen how the noise spectral density is multiplied by the NTF (H(f)).

\[ N_o^2 = \int_{0}^{f_b} E^2(t) \, df = e_{\text{rms}}^2 \frac{2f_b}{f_s} = e_{\text{rms}}^2 / \text{OSR} \]  

(2.3)

Using (eq. 2.4) a linear model prediction for the expected signal-to-noise ratio (SNR) can be made for the AZ modulator:

\[ \text{SNR} = S - N_o^2 \quad (\text{dB}) \]

\[ = S - 10 \log \left( \frac{\Delta^2}{12} \right) - 10 \log \left( \frac{1}{\text{OSR}} \right) - 10 \log \left( |H|^2 \right) \]

(2.5)

where: \( S \) is the signal power in dB

2.1.1.2 **Positioning the Band**

The location of the NTF zeros (filter poles) will determine the band of frequencies that the quantization noise will be filtered away from. To design a LPΔΣ A/D converter the NTF zeros would be placed around DC in order to push quantization noise away from DC. If a BPΔΣ A/D converter is desired the NTF zeros are placed at the frequency that the quantization noise should be filtered away from. To illustrate, the pole-zero location and resulting output spectrum of a 3\textsuperscript{rd}-order LPΔΣ modulator is shown in Fig. 2.3 and the equivalent 6\textsuperscript{th}-order BPΔΣ modulator in Fig. 2.4. In both modulators the NTF zeros were spread throughout the band of interest to maximize noise suppression[10].

With BPΔΣ modulation the designer is usually given the centre frequency \( (f_o) \) of the band of interest. Where this band is placed in the z-plane is usually set by the maximum
sampling rate obtainable in the given process. The benefits of using the maximum sampling frequency possible are a larger transition band and a higher OSR. A large transition band greatly reduces requirements on the anti-aliasing filter, and a higher OSR makes it possible to meet required resolution with a lower order modulator. Another consideration in placing the band is the decimation side of the ΔΣ A/D converter. At certain band placements, such as \(\theta = 2\pi \left( f_\text{o} / f_s \right) = \pi / 2 \) or \( \pi / 4 \), some innovative circuit design and decimation techniques are possible. This aspect of placing the band will be discussed in section 2.1.2.2.
2.1.1.3 Modulator Order

The order of the modulator and OSR have been related to SNR in previous work. For \( \text{LP\Delta}\Sigma \) modulators, an increase in SNR of approximately \((6N + 3)\) dB can be obtained for every octave increase in OSR (N is the order of the modulator)[9]. In \( \text{BP\Delta}\Sigma \) modulators the increase in SNR is \((3N + 3)\) dB/octave[11]. The reason for the difference is that in \( \text{BP\Delta}\Sigma \) modulators there are only \( N/2 \) NTF zeros in-band whereas with \( \text{LP\Delta}\Sigma \) modulators there are \( N \) zeros in-band.

Simulated results for 4\textsuperscript{th}-, 6\textsuperscript{th}-, and 8\textsuperscript{th}-order \( \text{BP\Delta}\Sigma \) modulators are shown in Fig. 2.5. (designed to meet the specification in Table 1.1) With the low OSR(33x), dictated by the specifications, large gains in SNR are not realized when going to higher-order modulators. Simulated results show an increase in SNR of 10dB when switching from a 4\textsuperscript{th}-order to a 6\textsuperscript{th}-order \( \text{BP\Delta}\Sigma \) modulator and only 5dB more when increasing to an 8\textsuperscript{th}-order \( \text{BP\Delta}\Sigma \) modulator. From these results, a 6\textsuperscript{th}-order \( \text{BP\Delta}\Sigma \) modulator would be required to meet the radio specifications of 12 bits. This modulator however, would be operating on the edge of stability. Therefore, a better choice to meet radio specifications would be an 8\textsuperscript{th}-order \( \text{BP\Delta}\Sigma \) modulator.

![SNR versus input amplitude for a 4\textsuperscript{th}-, 6\textsuperscript{th}-, and 8\textsuperscript{th}-order \( \text{BP\Delta}\Sigma \) modulator. (OSR = 33x)](image_url)
2.1.2 Decimation

As shown in Fig. 2.3b and Fig. 2.4b the output bit stream from the modulator not only contains information about the input signal but also contains large amounts of out-of-band energy: modulation noise. The objective of decimation is to attenuate all of this out-of-band energy with a digital filter such that when the signal is re-sampled at the Nyquist rate it will not be degraded significantly by noise aliasing back into the signal band.

2.1.2.1 Lowpass Decimation

There are several good papers on decimating the output of \( \text{LPA\Sigma} \) modulators. Two of the more popular choices are the \( \text{sinc}^k \) approach used in [9] and the brute force \( \text{ROM} \)-based FIR decimation scheme described in [12].

2.1.2.2 Bandpass Decimation

The obvious way to decimate the output of the \( \text{BPA\Sigma} \) modulator would be to build a narrowband digital filter. This might be quite challenging and expensive. A simpler approach, introduced in [13], would be to mix the output of the modulator down to baseband and then use conventional decimation means. The mixing stage can be greatly simplified if the centre frequency \( f_0 \) of the modulator is a simple fraction of the sampling frequency \( f_s \). For example, if \( f_0 = f_s / 4 \) then to mix the signal down to baseband one would only require the output of the modulator be multiplied by a simple periodic sequence given in (eq. 2.6).

\[
e^{-j f_0 t} = (1, 0, -1, 0, \ldots) + j (0, -1, 0, 1, \ldots)
\]

(2.6)

The resulting product would be just a pair of interleaved bit-streams, each with a bit rate of \( f_s / 2 \). These streams would then be lowpass filtered and down-sampled using conventional means.
2.2 Implementation of $\Delta\Sigma$ modulators

Methods of implementing the $\Delta\Sigma$ modulator can be grouped into 2 categories: continuous-time and discrete-time. These categories correspond to the method used to realize the loop filter used in the $\Delta\Sigma$ modulator.

The continuous-time approach, such as inductor-[3][14] or transconductor-based technologies, have the advantage that they do not require a sample-and-hold circuit. This operation is performed at the input to the quantizer and, as a result, any error that is made in the sampling process will get noise shaped. In the same breath it should be noted that the D/A converter, in the feedback loop of the modulator, now has to generate very accurate pulses. Any error in these pulses (due to clock jitter, for example) will seriously degrade the performances of the $\Delta\Sigma$ A/D converter.

The discrete-time approach, such as switched-C technology[1][2], has the advantage of being able to realize very accurate filters without the need for tuning. The main argument against implementation in discrete-time is the requirement of a sample-and-hold (S/H) circuit operating on a very fast input signal. However, S/Hs operating at sampling rates of 50MHz with 13 bit accuracy have been reported (implemented in a 1.2μm CMOS process)[15].

Continuous-time techniques can be expected to dominate at very high frequencies, but it is uncertain at what frequency this transition will occur (one of the objectives of this thesis).

2.2.1 Topologies

The single stage topology has already been shown in Fig. 2.1. One of the problems with the single stage topology is that if the order of the noise shaping is higher than 2nd-order (LP$\Delta\Sigma$ or 4th-order BP$\Delta\Sigma$) there is no guarantee that the resulting system will be stable. Another approach to obtaining high-order noise shaping is to use multi-stage noise shaping (MASH) [16]. The basic principle of this topology is to use a second $\Delta\Sigma$ modu-
lator stage to digitize the error from the first ΔΣ modulator stage. The output of the second modulator can then be passed through a digital filter and subtracted from the output of the first stage modulator to leave quantization noise which has been filtered by the product of two NTFS. This is shown in Fig. 2.6. The main disadvantage of the MASH topology is that it relies on the matching of an analog filter and a digital filter to cancel the quantization error from the first stage. This is made quite complicated when the zeros are spread through the band of interest as those shown in Fig. 2.3 and Fig. 2.4. The digital filter $H_1(z)$ can no longer be realized by just simple delays but would require multi-bit coefficients. For this reason a single stage topology was chosen for our implementation.

2.3 Summary

The operation of the ΔΣ A/D converter was reviewed and a comparison of the lowpass and bandpass ΔΣ A/D converters made.

It was shown that to meet radio specifications with a 1-bit quantizer an 8th-order BPΔΣ modulator would be required. This modulator gave approximately 80dB SNR just before it went unstable. This result means a very good automatic-gain-control circuit would be required to keep the input signal small enough so the modulator doesn’t go unstable but yet large enough to obtain an SNR of 72dB (12 bits). It was concluded that
for the low $\text{OSR}(33x)$ a higher-order modulator would not enhance SNR significantly for the added complexity.

Switched-C technology was chosen for the implementation of the $\text{BPAΣ}$ modulator since this technology has been proven to produce high resolution at baseband and because it is a monolithic technology capable of delivering precision analog performance.

Higher-order single stage modulators have been known for instability but the matching required from the analog and digital filters used in MASH modulators was considered to be too difficult for $\text{BPAΣ}$ modulation, where more complex filters are required. Stability and higher-order single stage modulators will be discussed further in the next chapter.
CHAPTER 3

Multi-Level $\Delta\Sigma$ A/D Converters

From the background chapter, it was concluded that an $8^{th}$-order 1-bit BPAZ modulator would be required to meet the specifications outlined in chapter 1. Stability, or more precisely lack of it, is probably the first thing that comes to mind when designing higher-order modulators. There are a number of ways of detecting and resetting an unstable modulator but these methods can add distortion to the output signal [9][17]. Another method for increasing the probability of obtaining a stable modulator is increasing the number of internal levels used in the A/D and D/A converters [18]. By doing this the magnitude of the noise power being fed back to the high-order loop filter is reduced. This approach can also add distortion to the output signal if methods for dealing with the non-linear D/A converter are not taken into consideration.

In this chapter the performance of multi-level BPAZ modulators is enhanced by using high gain noise transfer functions (NTF). It will be illustrated through simulated results that a great deal of “stability” is gained by using multi-level A/D and D/A converters. Methods for dealing with non-linearities in the multi-level D/A converter will also be discussed and the resulting NTF for a 3-level $8^{th}$-order BPAZ modulator given.

3.1 High Gain Noise Transfer Functions

A rule of thumb that has been followed in the design of $\Delta\Sigma$ modulators says that to realize stable modulators the maximum gain of the NTF should be less than 2 [19]. This was shown to be incorrect [20]. The reason for wanting to increase the maximum gain of the NTF is the large increase in inband attenuation that can be realized [18][21]. It will be
shown in the next section that by increasing the maximum gain of the NTF the probability of the modulator being unstable also increases.

Using the software package filterX [10] several different 8th-order NTFs were obtained for the specifications outlined in Table 1.1. Within filterX there is an optimization routine that allows the user to place more importance (higher weighting) on certain aspects of the NTF than others [11]. By applying more weighting on the in-band performance than the out-of-band performance, some NTFs were able to obtain much better in-band attenuation by sacrificing out-of-band gain (maximum gain) (Fig. 3.1). To explain why increasing the maximum gain of the NTF would increase in-band attenuation might be possible through investigation into the Cauchy integral theorem [22], but this was considered to be outside the focus of this thesis.

3.2 $\text{BP\Delta \Sigma}$ Modulators with High Gain NTFs

Several NTFs of different order and maximum gain were designed and used with a 1-bit quantizer to form a $\text{BP\Delta \Sigma}$ modulator. Simulated results show that the maximum gain of the NTF could not be increased significantly before the higher-order systems
(order > 4) went unstable’ (Fig. 3.2). Therefore, to take advantage of the large increase in in-band attenuation from slight increases in maximum gain, the magnitude of the noise power being fed back to the modulator has to be reduced. The obvious way to do this is to increase the number of levels in the internal A/D and D/A converters. For this section the D/A converter is assumed to be ideal.

A number of different 8th-order NTFs were designed with various maximum gains. These NTFs were used with a variety of quantizers to produce a wide range of multi-level 8th-order BPΔΣ modulators. Simulated results given in Fig. 3.3 show that a much larger gain in SNR can be obtained when going from a 2-level quantizer to a 3-level quantizer, than just the 3.5dB which is obtained from reducing the quantization noise power. This extra gain in SNR is termed “added stability” and by taking advantage of it, in the 3-level system, the maximum gain of the NTF could be increased by 3dB resulting in a 15dB deeper notch: an 18dB increase in SNR over the 2-level system. By adding more quantization levels the maximum gain of the NTF can be increased further with increasing added

1. Instability is illustrated by the sharp fall off of the line connecting simulated results
stability. However, as will be shown in the following section, the resolution of the internal D/A converter will limit the modulator to approximately 12 bits. Therefore to select the desired NTF three things should be considered: the resolution required from the ΔΣ A/D modulator, the best resolution expected from the internal D/A converter and how many levels are desired to give the sense of security that the resulting modulator will be stable. Hopefully this will be made clearer in the following example:

Example: Say the D/A converter being used is accurate to 15 bits (90dB) and the modulator required should be as accurate as possible. Then from Fig. 3.3 it is seen that a 2-level system would not meet these requirements. A 3-level system with a NTF that has a maximum gain of 7dB would meet the requirements but it would be getting close to the edge of stability. Therefore a good choice for the modulator would be a NTF with a maximum gain of 7dB and a 5-level quantizer.

The possibility of using a lower-order multi-level modulator to meet the radio specifications was also investigated and several different modulators appear in Figure 3.4. Each modulator uses a 3-level quantizer and a NTF that has its maximum gain increased until the modulator goes unstable. From these results a 6th-order modulator with a maximum
gain of 6dB would give a SNR value of approximately **75dB** which would meet radio specifications but with very little safety margin. Therefore an **8th-order** modulator will be required.

### 3.3 Linearity Problems with the D/A Converter

As mentioned in the background chapter, the D/A converter being used in the feedback loop needs to be as accurate as the overall ΔΣ A/D converter. Errors in the linearity of the D/A converter will not only limit the accuracy, but can also generate harmonic distortion in the output of the modulator. From simulation results however, it was observed that in a **5-level** system the outer levels were not used as often as the inner levels. If a fully differential circuit is used it is conceivable that the inner three levels could be designed to match quite closely (say better than 0.01%) [23]. Then the mismatches in the outer levels would only inject error into the system occasionally since they are only being used occasionally. Errors were made in the outer levels of the **5-level** D/A converter and the net result is shown in Figure 3.5b. Even though the outer levels do not get used very
### FIGURE 3.5  **In-band spectrum of a 5-level 8th-order BPΔΣ modulator.**

(input at -6dB)

- a) Ideal 5-level D/A converter
- b) 0.1% error in outer levels of the 5-level D/A converter

often they severely grade the performance of the modulator by increasing the noise floor by 20dB and also increasing the harmonic content.

### 3.3.1 Randomizing the levels in the D/A Converter

Harmonics (Fig. 3.5b) generated by the non-linear D/A converter can be removed by randomizing the inner levels of the D/A converter [24]. In this method, the inner levels of the D/A converter are set by randomly selecting a subset of unit capacitors (the two outer levels are set by either selecting no unit capacitors or all the unit capacitors). As a result of this randomizing, the harmonics generated by the non-linear D/A converter are converted into white noise spread from 0 to \( f_s/2 \) (Fig. 3.6a). Unfortunately, in low OSR systems a large portion of this white noise will be in-band raising the noise floor resulting in a low SNR. Other methods for selecting unit capacitors do exist [25] but are not well suited for low OSR (< 64) either. (Fig. 3.6b).
FIGURE 3.6 Converting the harmonic distortion which was generated by the non-ideal D/A converter into white noise. Simulated results for the 5-level 8th-order BPΔΣ modulator which has 0.1% error in the D/A's inner levels. (input at -6dB)

a) selecting levels randomly  
b) using a look up table to select levels

3.4 3-level 8th-Order BPΔΣ Modulator

The added stability gained from using a 5-level quantizer was considered not to be worth the added complexity of the randomizer and 5-level decimation. Instead, a 3-level quantizer was considered to be acceptable, since in a differential circuit 3-levels can be obtained very accurately with careful circuit design and layout. Therefore, to meet the specifications outlined in Table 1.1, a 3-level 8th-order BPΔΣ modulator was selected. The resulting NTF is shown in Fig. 3.7 and is given in coefficient form in (eq. 3.1). The maximum gain of the NTF is 5dB which is 3dB less than can be used with a 3-level quantizer before it goes unstable (Fig. 3.3). Actually a 2-level quantizer might work with this NTF as well, which may allow some flexibility in the design of the D/A converter (have the “0” level selectable). A signal transfer function (STF) was also obtained from filterX (eq. 3.2). The poles of the STF are the same as the poles of the NTF to save on hardware, but the zeros are different. The output spectrum of the resulting modulator is shown in Fig. 3.8. A SNR of 87dB is obtained for a -6dB input, which allows a large safety margin.
\[ \text{NTF} = \frac{Y(z)}{N(z)} = \frac{b_0 + b_2 z^2 + b_4 z^4 + b_6 z^6 + b_8 z^8}{d_0 + d_2 z^2 + d_4 z^4 + d_6 z^6 + d_8 z^8} \]  
(3.1)

where:
\[
\begin{align*}
    b_0 &= b_8 = 1 & d_0 &= 0.33052 \\
    b_2 &= b_6 = 3.99171 & d_2 &= 1.64016 \\
    b_4 &= 5.98342 & d_4 &= 3.18569
\end{align*}
\]

\[ \text{STF} = \frac{Y(z)}{U(z)} = \frac{a_1 + a_2 z^2 + a_3 z^3 + a_5 z^5 + a_6 z^6 + a_7 z^7}{d_0 + d_2 z^2 + d_4 z^4 + d_6 z^6 + d_8 z^8} \]  
(3.2)

where:
\[
\begin{align*}
    a_1 &= -0.04775 & a_4 &= 0.04775 \\
    a_2 &= 0.00013133 & a_5 &= -0.00013133 \\
    a_3 &= -0.037990 & a_6 &= 0.037990
\end{align*}
\]

FIGURE 3.7  
Magnitude plot of an 8th-order NTF and a 7th-order STF (different zeros, same poles).

### 3.4.1 3-level Decimation

The complexity of decimating a 3-level signal is not much greater than that of a 2-level signal. In a 3-level system all that is required in the accumulator stage is the flexibility to add the digital filter coefficient, subtract the digital filter coefficient or do nothing. However, if the 3-levels can not be obtained to the required resolution on the analog side a slightly more complicated decimation structure could be used which contains digital error correction for 3-levels[42].
3.5 Summary

This chapter illustrated, through simulation results, the benefit of using a multi-level quantizer to enhance the performance of the $\Delta \Sigma$ modulator. At the beginning of this work it was expected that the non-linearity in the D/A converter would be dealt with by using a randomizer to convert non-linearity in the D/A converter into white noise [24]. The randomizing approach did convert the harmonics generated by the non-linear D/A converter into white noise but for low OSR systems, a large portion of this white noise lies in-band greatly reducing SNR. Therefore, it was decided to use a 3-level quantizer with an 8th-order NTF that had a maximum gain of 5dB. The stability of this modulator is still not guaranteed, but the probability of the system being stable is greatly improved over a 2-level system.
To meet the sampling rate required for the A/D converter described in Chapter 1, some very fast circuits need to be designed. For \( \Delta \Sigma \) modulators, there is the added complexity of requiring analog and digital circuitry on the same chip. This problem is alleviated by the use of a BiCMOS process which is capable of delivering very fast bipolar devices for the analog modulator and very dense CMOS for the decimator.

In this chapter, the building blocks that will be used in the design of a pair of 1-bit 2nd-order \( \Delta \Sigma \) modulators, detailed in Chapter 5, are discussed. The circuits are designed in a 0.8\( \mu \)m BiCMOS process [26](\( \pm 2.5 \)V) and include a fully differential OTA with continuous-time CMFB, a pseudo-ECL comparator, switches, a clock generator, a D/A converter, and a sample-and-hold.

### 4.1 Operational Amplifier Design

Requirements of the operational amplifier used in the AZ modulator are well matched to the performance obtainable from a fine-line silicon process. A DC gain greater than 55dB [30][31] and unity-gain bandwidth of approximately 5 times the sampling frequency [32] are required to prevent modulator performance degradation. The DC gain requirement is low enough to be matched with a single stage topology, which makes it easier to meet the bandwidth requirement. Although there are several different single stage topologies that could be used to meet these requirements, the folded cascode OTA was considered to be the most robust.

A fully differential folded cascode OTA with continuous-time common-mode feed-
back was designed (Fig. 4.1). An infinite input impedance was required for the switched-C filters to avoid charge leakage, so MOS inputs were used. PMOS devices were selected so that the much faster NPN bipolar devices could be used as the current buffers (Q1, Q2) where the second pole occurs:

$$P_2 = \frac{g_{m,Q1}}{c_{\pi,Q1} + (c_{dg} + c_{ds} + c_{db})_{M1}} \quad (4.1)$$

The second pole ($P_2$) is now at a much higher frequency than normally obtained with a pure CMOS OTA. This allows a much higher unity-gain frequency without sacrificing phase margin.

A continuous-time CMFB circuit was chosen over a switched-C version[33] because continuous-time was considered to be a more reliable method. Continuous-time CMFB is also faster since in the switched-C version an extra capacitor is required to sense the output voltage and this would appear as a load to the differential path, decreasing the OTA bandwidth. The common-mode feedback circuit shown in Fig. 4.1 is very similar to the
pure CMOS version found in [34]. In our design however, the output voltage of the OTA is sensed with a pair of emitter followers rather than source followers. This makes the sensing process faster and more linear. The common-mode voltage is determined through a pair of resistors (R) and bypass-capacitors (C). Once the common-mode voltage in the output is determined it is compared to a reference and the error is amplified and fed back to the OTA via a current mirror which has a gain of 2. The value of R was chosen such that; at DC the impedance looking into base of Q3 \((R_{\text{in}} = \beta R)\) would be 10 times larger than the output impedance of the OTA. Capacitor C was chosen such that the pole created by R and C (eq. 4.2) would be roughly 10 times higher than the dominant pole of the OTA \((1/R_o C_{\text{Load}})\).

\[
Z_{\text{in}} = (r_\pi + (\beta + 1) R) \left( \frac{1 + s R}{1 + s R} \right) \left( \frac{1 + s R C}{1 + s R C} \right)
\]

bias voltages used in the OTA were generated using the circuit shown in Fig. 4.2. An off-chip resistor was used to set the current to approximately 300\(\mu\)A. The design allows optimal swing at the output of the amplifier. Bias voltage \(V_{b3}\) is 1.5\(V_{be}\) above \(V_{ss}\) and \(V_{b2}\) is \((V_U + 2V_{eff})\) below \(V_{dd}\). This allows the output of the folded cascode OTA to swing linearly between \((V_{be} - V_{ss})\) and \((V_{dd} - 2V_{eff})\).

**Figure 4.2** Biasing circuit for the folded cascode OTA

\[R_{\text{ext}} = 8.5k\Omega \]
\[R = 5k\Omega \]
\[a = 125/1 \]
\[x = \text{NN52111X}\]
The frequency response of the folded cascode OTA for different load capacitors is shown in Fig. 4.3. This figure illustrates how the single stage amplifier is load-capacitor-compensated. The second pole is at approximately 3GHz which allows the output capacitance to be quite small and still obtain satisfactory phase-margin. Settling time was determined by connecting the OTA as shown in Fig. 4.4 and applying a step to the input. Simulated results for two different capacitor values are shown in Fig. 4.5.

FIGURE 4.3 Frequency response of the folded cascode OTA

FIGURE 4.4 Test configuration for measuring settling time
A summary of the simulated results for the folded cascode OTA is given in Table 4.1. Both the DC gain requirement and unity-gain bandwidth requirement that were set out in the first paragraph of this section have been met. The settling time to 0.1% does seem to be quite long (9.0ns) considering that one half the clock period at 80MHz is only 6.25ns. However, it was uncertain at this time if 0.1% settling of the OTA output was requited when used in a bandpass ΔΣ modulator. In section 5.1.5 the effects of finite OTA settling on the performance of the modulator will be studied in detail.

**TABLE 4.1** Simulated results of the Folded Cascade Amplifier

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain</td>
<td>57dB</td>
</tr>
<tr>
<td>Unity-gain frequency</td>
<td>500MHz</td>
</tr>
<tr>
<td>Phase-margin</td>
<td>75°</td>
</tr>
<tr>
<td>*Settling time to 0.1%</td>
<td>9.0ns</td>
</tr>
<tr>
<td>Slew-rate</td>
<td>1000V/μs</td>
</tr>
<tr>
<td>Differential output range</td>
<td>5.2V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>26mW</td>
</tr>
</tbody>
</table>

measurements for a 1pF load capacitor

*measured as shown in Fig. 4.4 with C_L = 0.6pF*
4.2 Comparator

The comparator (Fig. 4.6) was a version of an existing part\[35\] modified by replacing bipolar inputs with NMOS devices to avoid loading the output of the OTA (which would reduce its gain and settling accuracy). **Internally** the comparator uses pseudo-ECL levels which are generated by the circuit shown in Fig.4.7a. The pseudo-ECL output levels from the comparator are then converted back to **TTL** levels by the inverters shown in Fig. 4.7b. The comparator has approximately 8 bit accuracy at 200\text{MHz}, which is sufficient for \(\Delta\Sigma\) modulators since \(\Delta\Sigma\) modulators are known to be tolerant of comparator offsets and **hysteresis** (any errors in the comparator see a high loop gain).

![Figure 4.6 Pseudo-ECL latched comparator](image)

4.3 Switches

A differential, parasitic insensitive, switching scheme that is used in the modulator filter is shown in Fig. 4.8 [36]. Signal dependent charge injection can be reduced by turning switch S4 off slightly before switch S 1 (1ns). As a result of this phasing arrangement, when S 1 is turned off it will see an infinite impedance to the right o...
FIGURE 4.7  Support circuitry for pseudo-ECL comparator
a) pseudo&CL clock level generator
b) pseudo-ECL to TTL converter

FIGURE 4.8  Switching and required clock phasing

itor C_{in} and hence the voltage across C_{in} will not change significantly. Switch S4 will still inject charge when it is turned off but this will be a constant amount that will appear only as a common mode-signal which will be rejected by the differential OTA. Switch S2 also goes off before S3, but in this case it is not because of signal dependent charge injec-
tion (because the signal on both sides of S2 will be quite small), but instead so the charge under the gate of S2 will split evenly, reducing its effect at the virtual ground of the input of the OTA.

A simple NMOS device would be sufficient for all the switches, since the charge injection in a differential circuit only appears as a common-mode component which would be rejected by the differential OTA. Even switch S1 could be a single NMOS device since the output of the OTA will (should) always be at least 1.2V below \(V_{dd}\) and the NMOS switch could pass all signals in this range. However, in practical differential circuits there will be mismatches between the two differential paths and the common-mode signal could be transformed into a differential signal. For this reason it was decided to use complementary transmission gates for all the switches to obtain charge cancellation (this point will be discussed further in section 4.7).

The switches were designed to have 7\(\tau\) settling in 5ns when connected to a 1pF load capacitance. With these specifications the maximum “on resistance” of the switch was determined to be 714\(\Omega\) (eq. 4.3).

\[
R_{on} = \frac{\tau}{C} = 714\Omega
\]  

The “on resistance” of the NMOS device which makes up half of the switch is given by (eq. 4.4).

\[
R_{on} = \frac{2}{\mu_n C_{ox} (W/L)(V_{gs} - V_t)}
\]  

Solving (eq. 4.4) for W/L and using the value of \(R_{on}\) derived in (eq. 4.3) (the “on resistance” of the parallel PMOS device was considered as an extra safety factor) the size of the NMOS switch is derived to be 15/0.8. However, there are two switches in series (S1, S4), therefore the size of the switch needs to be doubled to get W/L = 30/0.8. The PMOS device was chosen to be the same size as the NMOS device in order to get charge cancellation.
4.4 Clock Generation

The multi-phase clock generator (Fig. 4.9) required for the switching scheme used in Fig. 4.8 was designed by modifying an existing, slower BNR clock generator. The modifications consisted of removing a number of delays between $\text{mr2p}$ and $\text{md2p}$ and moving the “cross over” point (A) from the output of $\text{td2p}$ to the output of $\text{tad2}$. With these changes the resulting clock generator was asynchronous, which meant care had to be taken in layout in order to match capacitive loading on each phase. Simulated results on the extracted clock generator (with parasitics and 0.75pF capacitive loading) are shown in Fig. 4.10. For both phases (phl, ph2) delayed versions (phld, ph2d) are also generated, which go “low” approximately 1 ns after the undelayed versions.

![Diagram of multi-phase clock generator]

FIGURE 43 Multi-phase clock generator

4.5 D/A Converter

For a 1-bit $\Delta \Sigma$ modulator the D/A converter is very simple. The only requirement is determining which reference voltage to feed back to the modulator.

1. Modifications to the BNR clock generator were made by Theodore Varelas.
In our design the output of the comparator \((Q, \overline{Q})\) is compared to the clock phase through two AND gates. The output of the AND gates are then used to switch in the required reference signal to be fed back to the modulator, as shown in Fig. 4.11.

FIGURE 4.11  Circuitry used in the D/A converter (solid lines)
4.6 Sample-and-Hold

Possibly the most difficult block of the switched-C \(BP\Delta\Sigma\) modulator is the sample-and-hold (S/H) circuit. Any error generated in the S/H circuit will be seen in the output. This means the S/H block must be as accurate as the over-all performance of the \(\Delta\Sigma\) A/D converter. This is made especially difficult in \(BP\Delta\Sigma\) modulation, as compared to \(LP\Delta\Sigma\) modulation, because the input signal is much closer to the sampling frequency. Example: for a \(f_s/4\) modulator the input signal could change by its peak voltage from one sample instant to the next. As a result any clock jitter would contribute significant error to the sampled input.

These problems do not appear to be life-threatening to the future of switched-\(BP\Delta\Sigma\) modulators. Techniques for reducing the effects of clock jitter in the band of interest have been reported \cite{37} and S/H circuits that can sample at 50MHz with 13 bit accuracy have been developed (1.2\textmu m CMOS process) \cite{15}.

No extra circuitry was designed for the S/H circuit at this time because the 2\textsuperscript{nd}-order modulators, implemented in the next chapter, were not expected to have a resolution greater than 8 or 9 bits. Therefore, a simple switch and capacitor, as shown in Fig. 4.8, will be sufficient.

4.7 Summary

The high-speed analog circuits required for the 2\textsuperscript{nd}-order \(BP\Delta\Sigma\) modulator prototypes, detailed in the next Chapter, have been discussed.

The folded cascode OTA was chosen for its robustness compared to other single stage topologies, however, it will be shown in the next section that the large parasitic input capacitance of the PMOS devices and poor slew rate increases settling time significantly.

The comparator was a simple modification to a very fast, power hungry existing part. It was selected because it was a proven working part, however, comparators that can operate at the same speed with 1/10 the power have been reported \cite{38}.
Transmission gates were used for all switches in our design. In simulations, where perfect device matching and an ideal clock generator are used, transmission gates are an effective way of achieving perfect charge cancellation. However, in real circuits this is not the case. The net effect with transmission gates is more total charge that needs to be cancelled [39]. To get good charge cancellation, both devices have to turn off at the same time and the device sizes need to match, both of which are process dependent. Therefore, in a differential circuit, a single NMOS device should be used wherever possible for the switch, and where large signals need to be passed the on resistance of the PMOS and NMOS devices should match rather than capacitance such that large and small signals will get passed equivalently.

The clock generator was a rushed modification of a slower BNR part. Although this part is fast enough, it could be improved upon by matching delays between barred and unbarred phases such that when one goes high the other goes low at the exact same time. A method for doing this is shown in [40].

The S/H circuit was a simple switch and capacitor for our biquad design. However to meet radio specifications a more sophisticated S/H will need to be designed. References to very fast S/Hs [15] that have the required accuracy were given for this purpose.
CHAPTER 5

2nd-Order Bandpass AZ Modulator Prototypes

In chapter 3 it was determined that an 8th-order BPΔΣ modulator with a 3-level quantizer was necessary to obtain the accuracy required for the ND converter described in chapter 1. At the time of this research, it was uncertain if switched-C circuits could operate at the required 80MHz; so rather than building an 8th-order modulator and simultaneously running into stability, multi-level quantizer and clock-rate problems, it was decided to test the new building blocks described in chapter 4 with a 2nd-order BPΔΣ modulator prototype and a simple one-bit quantizer. The main interest was to push the sampling frequency as high as possible to determine the maximum practical sampling rate and the limiting factors. This prototype, after being tested and possibly revised, could then be cascaded to obtain the 8th-order BPΔΣ modulator required for the A/D converter.

This chapter presents the design, implementation, and test results of two different types of 2nd-order switched-C BPΔΣ modulators. Both structures use the same building blocks but employ different clock phasing with different trade-offs between active and passive sensitivities. The effects of capacitor mismatches and non-ideal OTAs on the performance of the modulators are also determined and compared to tested results.

5.1 Designing the Prototypes

Both 2nd-order prototypes have one NTF zero at (1/4)f_s. With just one zero in-band, it is quite easy to track the location of the notch frequency and its depth. Any errors in the location of this notch frequency due to finite OTA gain and capacitor mismatches can be determined by looking at the spectrum of the output bit stream at fairly low clock
rates (where the OTA is guaranteed enough time to settle). Once these errors are determined the clock frequency can be increased and the effects of incomplete OTA settling on the location of the notch frequency determined.

As explained in chapter 2, the poles of the loop filter (zeros of the NTF) determine the band of frequencies from which the noise will be filtered away. Therefore, to obtain a notch at \((1/4)f_s\), the desired filter response is:

\[
A(z) = \frac{1}{z^2 + 1}
\]

which results in a noise transfer function \(H_q(z)\):

\[
H_q(z) = \frac{z^2 + 1}{z^2}
\]

Ideally, to obtain the largest SNR possible, it is desirable to have the magnitude of the NTF zero exactly equal to 1 and its angular frequency exactly in the centre of the band of interest which, in our design is at \(\pi/2\). Any error in either one of these quantities, due to capacitor errors or non-ideal OTAs, will increase the amount of quantization noise in the band selected for decimation. Since certain filter structures are better at obtaining an accurate filter pole magnitude, while others are better at obtaining an accurate filter pole angle when faced with circuit non-idealities, it was considered interesting to see which affected SNR more severely. To determine how sensitive the SNR is to non-ideal NTFs, slight errors in the magnitude and angle of the NTF zero were made and the SNR calculated using the linear model. The results (Fig. 5.1) show that SNR is more sensitive to errors in the angle of the NTF zero than errors in its magnitude. However, magnitude errors can result in dead bands and limit cycles which would not appear in the linear model [20]. In higher order system dead bands and limit cycles are not much of a problem because there are many different states which help to randomize the input into the quantizer and break up these effects [28]. Also shown in Fig. 5.1 are the results of using two different OSRs: lower oversampling-ratio system are more tolerant of errors in the location of the NTF.
Several different biquad structures can be used to realize the filter response given in (eq. 5.1). In the following sections two different structures are compared. The first to be discussed is the lossless discrete integrator (LDI) phased modulator. As will be shown, the LDI modulator is more demanding on the speed of the OTAs but is capable of delivering infinite Q filters in spite of capacitor mismatches. The second switching scheme to be discussed is the Forward Euler (FE) phased modulator which is tolerant of slightly slower OTAs but in which the Q of the filter is dependent on capacitor matching.

### 5.1.1 LDI Modulator

The LDI modulator is shown in Fig. 5.2. The comparator was replaced by a linear white noise source and a delay, which is used to represent the one clock cycle that is required for the comparator. The filter is shown within the dashed lines of Fig. 5.2. Phasing of the integrators was selected such that the OTAs settle in parallel rather than series. In this way one OTA will never have to wait for the other OTA to settle. As seen in Fig. 5.2, the input signal \( U(z) \) and the noise signal \( N(z) \) can see slightly different filter responses (same filter poles but different filter zeros) by appropriately choosing feed-in and feed-back capacitors \( C_a \)s and \( C_b \)s. To keep it as simple as possible the same filter
FIGURE 5.2 Singled-ended representation of the LDI modulator

response (eq. 5.1) was chosen for both.

The filter response \( A_N(z) \) that the quantization noise sees is given by (eq. 5.3).

\[
A_N(z) = \frac{X(z)}{Y(z)} = \frac{C_{b0} C_x}{C_{i1} C_{i2}} - \frac{C_{b1}}{C_{i2}} (z - 1)
\]

\[
z^2 - \left( 2 + \frac{C_r}{C_{i1} C_{i2}} \right) z + 1
\]

Setting (eq. 5.3) equal to (eq. 5.1) and capacitors \( C_{i1} = C_{i2} = C_x = 1 \) the remaining capacitor values can be determined: \( C_{b0} = 1 \), \( C_{b1} = 0 \) and \( C_r = -2 \). The negative capacitance value for \( C_r \) is not a problem since fully differential circuits are being used and the negative sign can be obtained by simply feeding the capacitor into the opposite side of the OTA. Similarly the feed-in capacitors for the input signal can be determined: \( C_{a0} = 1 \) and \( C_{a1} = 0 \).

The location of the filter poles is determined by setting the denominator of (eq. 5.3) equal to zero and solving for \( z \). The solutions are given in (eq. 5.4) with the magnitude of the filter pole given in (eq. 5.5) and its angle in (eq. 5.6).

\[
z = 1 + R/2 \pm j \sqrt{-(R + R^2/4)}
\]

\[|z| = 1\]
\[ \angle z = \arctan \left( \frac{\sqrt{-R^2/4}}{1 + R/2} \right) \]  

where:  
\[ R = \frac{C_r C_x}{C_{i1} C_{i2}} \]

With ideal OTAs the LDI structure guarantees that the filter pole will have a magnitude of 1, independent of capacitor ratios. Location of the notch frequency is derived from the angle of the filter pole (eq. 5.6) and is given below:

\[ f_{\text{notch}} = \frac{f_s}{2\pi} \arctan \left( \frac{\sqrt{R^2/4}}{1 + R/2} \right) \]  

(5.7)

From (eq. 5.7) the error in the notch frequency \( \Delta f_{\text{notch}} \) due to capacitor mismatch can be determined. Assuming \((1 + R/2) \ll 1\) the error in the notch frequency becomes:

\[ \Delta f_{\text{notch}} = \frac{f_s}{2\pi} (1 + R/2) \]  

(5.8)

which means four different capacitors (R) can contribute to errors in the location of the notch frequency. Simulated results for capacitor mismatch vs. pole frequency are given in section 5.1.4.

5.1.1.1 OTA Loading in the LDI structure

The luxury of having the magnitude of the filter pole independent of capacitor ratios in the LDI structure comes with the drawback of “unbalancing” the capacitive loading seen by the unbuffered OTA. Capacitive loading on the OTA for the different clock phases is shown in Fig. 5.3.

![Capacitive loading seen by OTA A2 in the LDI structure on each clock phase. (Cp and Cip are the input and output parasitic capacitances of the OTA)](image)
During phase 1 the input and output capacitors are connected to the OTA, and on phase 2 the OTA is left floating. Using feedback analysis methods the OTAs closed-loop time constant can be easily derived.

![Block diagram of OTA in feedback.](image)

**FIGURE 5.4** Block diagram of OTA in feedback.

The gain of the OTA with feedback is given in (eq. 5.9).

\[
A_f = \frac{A}{1 + \beta A}
\]  

(5.9)

Assuming the OTA has a single pole “roll off” (\(A = \omega_l / s\)) the closed-loop frequency response becomes:

\[
A_f = \frac{\omega_l}{s + \beta \omega_l}
\]  

(5.10)

From (eq. 5.10) the closed-loop time constant \(\tau\) of the OTA is derived.

\[
\tau = \frac{1}{\beta \omega_l}
\]  

(5.11)

During phase 1 the feedback factor is going to be less than 1 (input capacitor is connected)

\[
\beta_{\theta1} = \frac{C_2}{C_1 + C_p + C_2}
\]  

(5.12)

and the unity gain frequency will be reduced (load capacitance is connected)

\[
\omega_{\theta1} = \frac{g_{m,\text{input}}}{C_3 + C_{p} + (C_1 + C_p)C_2/(C_1 + C_p + C_2)}
\]  

(5.13)

resulting in a large closed loop time constant.

During phase 2, when input and output capacitances are disconnected, the feedback factor will be larger:
\[ \beta_{\theta_2} = \frac{C_2}{C_p + C_2} \]  

(5.14)

and \( \omega_1 \) will be larger:

\[ \omega_{\theta_2} = \frac{g_{m,\text{input}}}{C_{lp} + C_p C_2 / (C_p + C_2)} \]  

(5.15)

resulting in a small closed-loop time constant.

This “unbalancing” of the capacitive load seen by the OTA results in a long settling time on one of the clock phases (phase one, in this case) reducing the maximum clock speed.

Example: Using the data for the folded cascode OTA described in chapter 4, namely \( g_{m,\text{input}} = 4 mA/V, C_p = 0.6 \text{pf}, C_{lp} = 0.3 \text{pf} \) and selecting \( C_1 = C_2 = C_3 = 0.6 \text{pf} \) the closed-loop time constant on phase 1 becomes \( \tau_{\theta_1} = 0.97\% \) and on phase 2 it becomes \( \tau_{\theta_2} = 0.45\text{ns} \).

Thus, due to unbalancing the capacitive load, this structure will require 6.83ns to obtain 7\( \tau \) settling (assuming the OTA does not slew).

### 51.2 FE M odulator

A single-ended representation of the FE modulator is shown in Fig. 5.5. The filter response that the quantization noise sees \( (A_N(z)) \) is given by (eq. 5.16).

\[ A_N(z) = \frac{X(z)}{Y(z)} = \frac{C_{b0}}{C_{i1}} C_x - \frac{C_{b1}}{C_{i2}} \frac{z - 1}{z^2} \left( 2 + \frac{C_d}{C_{i1}} \right) z + \left( 1 - \frac{C_x}{C_{i1}} \frac{C_{i2}}{C_{i1}} \right) \]  

(5.16)

\[ U(z) \]

\[ C_{a0} \]

\[ C_{i1} \]

\[ C_x \]

\[ A_1 \]

\[ C_{i2} \]

\[ C_{b1} \]

\[ C_{r} \]

\[ A_2 \]

\[ C_{d} \]

\[ N(z) \]

\[ X(z) \]

\[ Y(z) \]

**FIGURE 5.5** Single-ended representation of the FE modulator
Setting (eq. 5.16) equal to (eq. 5.1) and choosing $C_{i1} = C_{i2} = C_x = 1$, as with the LDI modulator, the capacitor values can be derived: $C_{b0} = -1$, $C_{b1} = 0$ and $C_r = C_d = -2$. Similarly $C_{a0}$ and $C_{a1}$ can be found to equal 1 and 0, respectively. Again the clock phasing was chosen so the OTAs settle in parallel rather than series. Setting the denominator of (eq. 5.16) equal to zero and solving for $z$ the poles of the filter are determined:

$$z = (1 + D/2) \pm j \sqrt{-(R + D^2/4)}$$

$$|z| = \sqrt{1 - R + D}$$

$$\angle z = \text{atan} \frac{\sqrt{-(R + D^2/4)}}{(1 + D/2)}$$

where: $R = \frac{C_r}{C_{i1}} \frac{C_x}{C_{i2}}$ and $D = \frac{C_d}{C_{i1}}$

The magnitude of the filter pole is dependent on capacitor ratios as shown in (eq. 5.18) which means that even with ideal OTAs an infinite Q filter is not guaranteed. Error in the notch frequency is derived assuming $|1 + D/2| \ll 1$.

$$\Delta f_{\text{notch}} = \frac{f_s}{2\pi} (1 + D/2)$$

The disadvantage of having the magnitude of the filter pole dependent on capacitor matching is countered slightly by the advantage of having the angle of the filter pole set mainly by the second integrator. This will be compared to the LDI modulator in section 5.1.4.

5.1.2.1 OTA Loading in the FE structure

An increase in integrator speed is realized with the FE clock phasing by “balancing” the capacitive loading seen by the OTA between the two clock phases as shown in Fig. 5.6. During phase 2 the input capacitance is connected to the OTA so the feedback factor is the same as that for the LDI modulator on phase 1 (eq. 5.12), but the output capacitance is not; the unity gain frequency (eq. 5.21) is much higher resulting in a small $\tau$. 

\[43\]
During phase 1 the output capacitance is connected which will reduce $\omega_t$ (eq. 5.22)

$$\omega_{t1} = \frac{g_m}{C_{ip} + C_p + C_3}$$

but, the input capacitance is not connected therefore the feedback factor will be larger (eq. 5.14) and $\tau$ will still be small. As a result of splitting up the capacitive loading on the OTA a smaller integrator tune constant is realized and faster clocking speeds should be obtainable.

**Example:** Using the data for the folded-cascade OTA described in chapter 4, namely,

- $g_{m, \text{input}} = 4\text{mA/V}$, $C_p = 0.6\text{pf}$, $C_{ip} = 0.3\text{pf}$
- selecting $C_1 = C_2 = C_3 = 0.6\text{pf}$

the closed-loop time constant on phase 1 becomes $\tau_{t1} = 0.6\text{ns}$ and on phase 2 it becomes $\tau_{t2} = 0.525\text{ns}$. Thus, as a result of balancing the capacitive load seen by the OTA, this structure will only require $4.2\text{ns}$ to obtain $7\tau$ settling (assuming the OTA does not slew). This is approximately 40% faster than the LDI structure.

### 5.1.3 Scaling Capacitors

For comparison, both modulator variants are shown simultaneously in their differential form in Fig. 5.7. Values and clock phasings for the FE circuit are shown in parentheses where the variants differ, and the sign inversion and additional “damping” capacitor needed for the FE case are shown connected with dotted lines. The negative capacitor values for $C_d$ and $C_r$ are obtained by connecting their bottom plates to the opposite side of
OTA $A_2$. The capacitors were scaled for maximum dynamic range (4 volt differential swing of the amplifiers) and their values are given in Table 5.1.

![Diagram of 2nd-order BPΔΣ modulators in their differential form](image)

**Figure 5.7** 2nd-order BPΔΣ modulators in their differential form
a) LDI modulator
b) FE modulator use clock phasing in () and dashed lines.

* TABLE 5.1 Nominal capacitor values for both modulator

<table>
<thead>
<tr>
<th>Component</th>
<th>$C_{b0}$</th>
<th>$C_{s0}$</th>
<th>$C_{i1}$</th>
<th>$C_{i2}$</th>
<th>$C_x$</th>
<th>$C_r$</th>
<th>$C_d^*$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value (pF)</td>
<td>0.2</td>
<td>0.2</td>
<td>0.5</td>
<td>0.3</td>
<td>0.5</td>
<td>0.6</td>
<td>0.6</td>
</tr>
</tbody>
</table>

* not present in the LDI modulator

### 51.4 Capacitor Mismatches

Assuming the OTAs used in the modulators are ideal, the effects of capacitor mismatch on the location of the filter pole can be determined by making slight errors to the capacitor values used in (eq. 5.8), (eq. 5.18) and (eq. 5.20). Errors were made to the two integrating capacitors and the resulting magnitude and angle of the filter pole determined and plotted in Fig. 5.8.

As earlier stated the magnitude of the filter pole with the LDI structure is independent of capacitor values. However, the angle of the filter pole with the LDI structure is approx-
imately twice as sensitive to capacitor error as the FE structure. This is intuitively satisfying since; in the LDI structure both integrators are used to place the angle of the pole whereas, in the FE structure only the second integrator is used.

5.1.5 Non-ideal OTAs

Effects of finite OTA gain, bandwidth and slew rate were considered when determining the equations that would predict the phase and magnitude errors in the two different biquads. The effects of finite gain and bandwidth on switch-C biquads, for zero output impedance op-amps, were previously investigated by Martin and Sedra [32]. These results were generalized to transconductance op-amps, where the transient due to charging amplifier loads is important, by Ribner and Copeland [41]. Neither of these analyses considered slew rate limited op-amps or input and output parasitic capacitances.

To determine the effects of non-ideal OTAs on the performance of the LDI modulator, the transfer function of the 1/2-delay non-inverting integrator using non-ideal OTAs must be determined. The ideal transfer function of the 1/2-delay non-inverting integrator is given by (eq. 5.23).

\[
\frac{V_o(z)}{V_i(z)} = \left(\frac{C_1}{C_2}\right) \frac{z^{1/2}}{z-1}
\] (5.23)
In the presence of non-ideal OTAs the integrator will have a gain error $P$ and pole error $M$ as shown in (eq. 5.24).

$$\frac{V_o(z)}{V_i(z)} = \frac{(C_1/C_2)P}{z^{1/2} - M}$$  \hspace{1cm} (5.24)

If the OTA has finite DC gain the value of $P$ and $M$ are given by (eq. 5.25)

$$P, M = 1 - \frac{(\kappa_{P,M})}{A_o}$$  \hspace{1cm} (5.25)

where $\kappa_P$ and $\kappa_M$ are constants related to capacitor values and $A_o$ is the DC gain of the OTA. If the OTA has finite bandwidth the value of $P$ and $M$ are given by (eq. 5.26)

$$P, M = 1 - (\hat{\phi}_{P,M}) e^{-\frac{1}{T}(t_{\text{settle}})}$$  \hspace{1cm} (5.26)

where $\hat{\phi}_{P,M}$ is a constant and $t_{\text{settle}}$ is the amount of time the OTA has for linear settling.

$$t_{\text{settle}} = T/2 - t_{\text{slew}} - t_{\text{overlap}}$$  \hspace{1cm} (5.27)

where: $T$ is the clock period

$t_{\text{slew}}$ is the amount of time the OTA spends slewing

$t_{\text{overlap}}$ is the time used up by the non-overlapping clock phases

The derivation of the constants in these equations involve using initial charge distribution at the instant the switch is closed. It is quite lengthy and resides in Appendix A. Also, due to the use of slew rate limited OTAs, which can produce intermodulation affects as well as frequency shifts, the equations to predict the errors are non-linear making the math quite difficult. Therefore, a linear approximation of the real behavior is made to simplify the final solution. The expected error in the filter pole magnitude and phase for the LDI modulator is given in Table 5.2.
TABLE 5.2 Effects of non-ideal OTAs on the LDI filter pole

<table>
<thead>
<tr>
<th>Description</th>
<th>Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnitude of filter pole</td>
<td>(</td>
</tr>
<tr>
<td>Phase error in filter pole</td>
<td>(\Delta \theta = \left(M_1 + M_2 - \frac{C_x C_x}{C_{i1} C_{i2}} (P_1 P_2)\right)/2)</td>
</tr>
</tbody>
</table>

Errors due to OTAs with finite DC gain use the following for \(M_n\) and \(P_n\):

<table>
<thead>
<tr>
<th>Description</th>
<th>Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>(M_1)</td>
<td>(1 - \frac{(C_r + C_a + C_b)/C_{i1}}{A_0})</td>
</tr>
<tr>
<td>(P_1)</td>
<td>(1 - \frac{(C_r + C_a + C_b + C_p + C_{i1})/C_{i1}}{A_0})</td>
</tr>
<tr>
<td>(M_2)</td>
<td>(1 - \frac{C_x / C_{i2}}{A_0})</td>
</tr>
<tr>
<td>(P_2)</td>
<td>(1 - \frac{(C_x + C_p + C_{i2})/C_{i2}}{A_0})</td>
</tr>
</tbody>
</table>

Errors due to OTAs with finite BW and SR use the following for \(M_n\) and \(P_n\):

<table>
<thead>
<tr>
<th>Description</th>
<th>Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>(M_1)</td>
<td>(1 - \beta_1 \xi_1 e^{-k_1})</td>
</tr>
<tr>
<td>(P_1)</td>
<td>((1 - \alpha_1 \xi_1 e^{-k_1}))</td>
</tr>
<tr>
<td>(M_2)</td>
<td>(1 - \beta_2 \xi_2 e^{-k_2})</td>
</tr>
<tr>
<td>(P_2)</td>
<td>((1 - \alpha_2 \xi_2 e^{-k_2}))</td>
</tr>
</tbody>
</table>

\(\beta_1 = \frac{C_x C_{e1}}{C_{w1} (C_{i1} + C_{ip} + C_x)}\), \(\xi_1 = \tau_1 (SR_1)/V_{max}\)

\(k_1 = \frac{1}{\tau_1} \left(\frac{1}{2 f_s} - \frac{V_{max}}{SR_1} + \tau_1^{-1} \tau_{overlap}\right)\), \(\alpha_1 = C_{e1}/C_{w1}\)

\(C_{e1} = C_r + C_a + C_b + C_p + C_{i1}\)

\(C_{w1} = C_r + C_a + C_b + C_p + (C_{ip} + C_x)\)

\(\tau_1 = \frac{C_{e1}}{C_{i1} \omega_{i1}}\), \(\omega_{i1} = \frac{\delta_m}{C_x + C_{ip} + C_{i1} (C_{e1} - C_{i1})/C_{e1}}\)

\(SR_1 = \frac{l_{bias}}{C_x + C_{ip} + C_{i1} (C_{e1} - C_{i1})/C_{e1}}\)

\(\beta_2 = \frac{C_r C_{e2}}{C_{w2} (C_{i2} + C_{ip} + C_x)}\), \(\xi_2 = \tau_2 (SR_2)/V_{max}\)

\(k_2 = \frac{1}{\tau_2} \left(\frac{1}{2 f_s} - \frac{V_{max}}{SR_2} + \tau_2^{-1} \tau_{overlap}\right)\)

\(\alpha_2 = C_{e2}/C_{w2}\), \(C_{e2} = C_x + C_p + C_{i2}\)

\(C_{w2} = C_r + C_p + C_{i2} (C_{ip} + C_r)\)

\(\tau_2 = \frac{C_{e2}}{C_{i2} \omega_{i2}}\)

\(\omega_{i2} = \frac{\delta_m}{C_r + C_{ip} + C_{i2} (C_{e2} - C_{i2})/C_{e2}}\)

\(SR_2 = \frac{l_{bias}}{C_r + C_{ip} + C_{i2} (C_{e2} - C_{i2})/C_{e2}}\)

... subscript \(n\) refers to integrator 1 or 2

... \(C_p\) is the input parasitic of the OTA

... \(C_{ip}\) is the output parasitic of the OTA

... \(SR\) slew rate

... \(\xi\) linear correction factor for slewing

... \(V_{max}\) maximum output step

The FE modulator consists of two 1-delay non-inverting integrators which have an ideal transfer function similar to (eq. 5.23) but with a full delay. The difference between the two types of integrators is that the 1-delay non-inverting integrator has transients occurring on both phases of the clock, one when the input capacitor is connected and another when the output capacitor is connected, whereas the 1/2-delay non-inverting inte-
The integrator only has one transient. Errors due to finite DC gain will be similar to the 1/2-delay non-inverting integrator but the errors due to finite bandwidth will be affected by incomplete settling on both phases. However, the integrator time constant is much faster for the 1-delay integrator on both phases. The non-ideal transfer function of the 1-delay non-inverting integrator is given by (eq. 5.28).

\[
\frac{V_o(z)}{V_i(z)} = \left(\frac{C_1}{C_2}\right) E \left(\frac{z^{1/2}}{z - F}\right)
\]

(5.28)

where: \( E = (1 - E_1)(1 - E_2) \)

\( E_1 \) and \( E_2 \) are the gain errors associated with phase 1 and phase 2.

\( F \) is the pole error in the integrator on phase 2 (negligible error on phase 1).

The values for \( E \) and \( F \) have been derived in Appendix A for both integrators in the FE structure. The summarized results are given in Table 5.3.

Using HSPICE simulation data obtained from chapter 4 for the OTA and the equations in Table 5.2 and Table 5.3, the magnitude and notch frequency error were determined for the two different modulators as the clock frequency was increased (Fig. 5.9).

![Figure 5.9](image)

**Figure 5.9** Effects of non-ideal OTAs on the performance of the LDI and FE modulators.

a) Magnitude of filter pole at different clock frequencies

b) Percentage error in notch frequency as clock frequency is increased
### Table 5.3: Effects of non-ideal OTAs on the FE Filter Pole

**Magnitude of filter pole**  \( \rightarrow |z| = \sqrt{\frac{C_x C_a}{C_{i1}} \left( E_1 E_2 \right)} - \frac{C_{d2} E_2 F_1}{C_{i2}} \)

**Phase error in filter pole**  \( \rightarrow \Delta \theta = \left( \frac{F_1 + F_2 - C_{d2} E_2}{C_{i2}} \right) / 2 \)

**Errors due to OTAs with finite DC gain** use the following for \( F_n \) and \( E_n \)

| \( F_1 \) | \( F_2 \) |
|\( 1 - \frac{(C_r + C_a + C_p) / C_{i1}}{A_0} \) | \( 1 - \frac{(C_x + C_d) / C_{i2}}{A_0} \) |

| \( E_1 \) | \( E_2 \) |
|\( 1 - \frac{(C_r + C_a + C_b + C_p + C_{i1}) / C_{i1}}{A_0} \) | \( 1 - \frac{(C_x + C_d + C_p + C_{i2}) / C_{i2}}{A_0} \) |

**Errors due to OTAs with finite BW and SR** use the following for \( F_n \) and \( E_n \)

| \( F_1 \) | \( F_2 \) |
|\( 1 - \beta_1 \tau_{1,1} e^{-k_{1,1}} \) | \( 1 - \beta_2 \tau_{2,2} e^{-k_{2,2}} \) |

| \( E_1 \) | \( E_2 \) |
|\( (1 - \alpha_1 \tau_{1,1} e^{-k_{1,1}}) (1 - \beta_1 \tau_{1,2} e^{-k_{1,2}}) \) | \( (1 - \alpha_2 \tau_{2,1} e^{-k_{2,1}}) (1 - \beta_2 \tau_{2,2} e^{-k_{2,2}}) \) |

\( \beta_1 = \frac{C_x (C_i + C_p)}{(C_x + C_{lp}) (C_{i1} + C_p) + C_{i1} C_p} \)

\( \alpha_1 = \frac{(C_r + C_a + C_b + C_p + C_{i1}) (C_{zp} + C_{lp})}{(C_{i1} + C_{zp}) (C_{i1} + C_p) + C_{i1} C_p} \)

\( \tau_{1,1} = \frac{\omega_{t,1,2}}{\beta_1 (C_i + C_p)} \), \( \tau_{1,2} = \frac{C_p + C_{i1}}{C_{i1} \omega_{t,1,2}} \)

\( k_{1,1} = \frac{1}{\tau_{1,1}} \left( \frac{1}{2 T_s} - \frac{1}{C_{LP1}} \right) \)

\( \omega_{t,1,1} = \frac{C_{i1} (C_r + C_x + C_b + C_p)}{C_{ip} + C_{i1} (C_r + C_x + C_b + C_p)} \)

\( \omega_{t,1,2} = \frac{C_x + C_{ip} + C_{i1} C_p}{C_{i1} C_x + C_b + C_p} \)

\( SR_{1,1} = \frac{I_{bias}}{C_{i1} (C_r + C_x + C_b + C_p) / C_{i1} C_b + C_p} \)

\( SR_{1,2} = \frac{I_{bias}}{C_x + C_{ip} + C_{i1} C_p / C_{i1} C_b + C_p} \)

\( \omega_{t,2,1} = \frac{C_{i2} (C_x + C_d + C_p)}{C_{i2} C_x + C_d + C_p} \)

\( \omega_{t,2,2} = \frac{C_x + C_d + C_{ip}}{C_{i1} C_x + C_d + C_p} \)

\( SR_{2,1} = \frac{I_{bias}}{C_{i2} (C_x + C_d + C_p) / C_{i2} C_d + C_p} \)

\( SR_{2,2} = \frac{I_{bias}}{C_x + C_d + C_{ip} + C_{i2} C_p / C_{i2} C_d + C_p} \)

...subscripts n.m refer to integrator n operating on phase m

...example: \( SR_{1,1} \) is the slew rate of integrator 1 when phase 1 is high.
5.2 Layout and Experimental Results

The circuits were implemented in a 0.8μm BiCMOS process [26]. Four different test configurations were laid out: folded cascode OTA, switched-C unity gain circuit, LDI modulator and FE modulator (Fig. 5.10).

FIGURE 5.10 Photomicrograph of test chip. (read counter-clockwise starting from the top left corner.)
  a) Folded Cascode OTA
  b) Unity gain switched-C test configuration
  c) LDI modulator
  d) FE modulator

5.2.1 Folded Cascode OTA

The DC gain of the folded cascode OTA was determined by applying a small sinusoid signal to the input of the OTA (open loop) and measuring the size of the sinusoidal output.
A DC gain of $55\text{dB}$ was obtained. The $g_m$ of the input devices was determined by placing a resistor across the two output terminals (Fig. 5.1a) and applying a small dc signal to the input of the OTA. Using (eq. 5.29) the $g_m$ of the input devices was calculated to be approximately $4\text{mA/V}$ which is the same as that obtained from Hspice simulations.

\[ g_m = \frac{2V_{out}}{RV_{in}} \]  

(5.29)

To determine the settling time, the folded cascode OTA was connected (on chip) in a unity gain switched-C configuration (Fig. 5.11b). Output buffers were added such that $50\Omega$ probes could be used for testing. The output buffers, emitter followers, had $2k$ resistors placed at the emitter such that the output of the OTA would not be loaded down by the $50\Omega$ probe. This resulted in a division by 40 in the output waveform. On phase 1, the input capacitors were charged to a DC voltage and the capacitors across the OTA were discharged. On phase 2, the input capacitors were connected to the OTA and the output rise time was measured. The rise time for the OTA was measured to be $3.3\text{ns}$. Assuming a single pole response the closed loop time constant was calculated to be $1.5\text{ns}$ using $t_r = 2.27$. This is a worst case estimate of what $\tau$ is since it does not take into consideration that the OTA is slewing for a portion of the rise time. However, it does give a lower limit to what the unity gain frequency of the OTA is:

\[ f_l = \frac{1}{2\pi\tau} > 318\text{MHz}(\text{at } \tau = 1\text{pF}) \]  

(5.30)
Each modulator was packaged and tested separately. The bit streams generated by the modulators were collected using a logic analyzer and saved to a data file for later processing. It should be noted that this is a much better approach than just taking pictures from an analog spectrum analyzer since the latter method will mask the effects of clock jitter. Fig. 5.12 shows the output spectrum of the LDI modulator when being clocked at 45MHz with two tones applied to the input. The two tone test shows very few intermodulation distortion products. This differs from the spectrum obtained from the FE modulator (Fig. 5.13) where many intermodulation distortion products are present (characteristic of finite pole Q [9][20][29]) but where the centre of the notch is much closer to 1/4 the sampling frequency.

Data were collected for both modulators at several different clock frequencies to see the effects of incomplete OTA settling on the location of the notch frequency. The results are plotted in Fig. 5.14 where the points are experimentally measured and the lines are mathematically predicted using the equations in Table 5.2 and Table 5.3. Below 20MHz the OTAs have enough time, after slewing, to settle linearly (greater than 7τ) and the errors in notch frequency are due to capacitor mismatch and finite OTA DC gain. Using
FIGURES 13 Output spectrum of the FE modulator when clocked at 45MHz. Two tone input each at -6dB.

a) output spectrum, abscissa contains 32768 bins
b) expanded view of in-band

FIGURE 5.14 Percentage error in notch frequency resulting from non-ideal OTAs. Points are experimentally measured and lines are mathematically predicted by equations in Table 5.2 and Table 5.3.

The measured DC gain of the OTA (55dB) and inserting this into the equations the capacitor mismatch was estimated to be -0.2% for \( C_{i1} \) and -0.3% for \( C_{i2} \). These are reasonable given that we are using small capacitor values. Shown in Fig. 5.15 is the SNR as the input changes in amplitude. The linear model predicts a lower SNR than measured results, which should not generate concern since the linear model assumes that the quantization
noise is white and in low order systems this is not generally the case \([9][27]\).

The experimental data used in determining the effects of incomplete OTA settling on the location of the notch frequency was also used in calculating the SNR in a 200kHz band centered at 1/4 the sampling frequency. Experimental results show that SNR increases by approximately 9dB/octave, as should be the case for 1st-order noise shaping, until incomplete OTA settling starts to affect the performance. This appears to happen between 20MHz and 30MHz for the LDI modulator and 35MHz and 45MHz for the FE modulator.
5.3 Summary

The objective of this chapter was to determine the maximum sampling speed obtainable from a switched-C \( \text{BP\Sigma} \) modulator and what the limiting factors would be. Two different structures were implemented to investigate this upper limit and were named the LDI modulator and FE modulator. The fact that the LDI modulator was capable of delivering an infinite Q filter in spite of capacitor mismatches made it an attractive architecture. However the reduced OTA bandwidth required by the FE structure made it very attractive as well even though the Q of the filter was dependent on capacitor matching. Experimental results showed that the FE modulator gave a speed advantage over the LDI modulator and the sensitivity of Q to capacitor errors did not appear to seriously degrade SNR. Higher order modulators are more tolerant to Q errors \[28\] so the FE modulator would be well suited for the required 8-th-order modulator.

The upper limit on the switched-C biquad was determined to be between 35MHz and 45MHz. The limiting factor in our design was the amount of time the folded cascode OTA required to settle. There were two major factors which contributed to this long settling time and they were the large parasitic input capacitance of the PMOS devices (0.6pf) and the large amount of time the OTA spent slewing the load capacitance (4.2ns). Methods of reducing both of these quantities will be discussed in section 6.2.
CHAPTER 6

Conclusions and Future Work

This chapter contains the conclusions that can be drawn from the work presented in this thesis. From these conclusions the direction that future work should take is discussed.

6.1 Thesis Conclusions

This thesis contributed to knowledge of architectural trade-offs in delta-sigma modulation, to high-speed BiCMOS analog circuit design, and to radio architecture.

Chapter 1 developed the motivation to perform A/D conversion at the IF stage of a radio. Specifications were obtained for a possible future digital radio from a report done by the Communications Research Centre. The main interest was in converting larger relative bandwidths to digital form to allow fine-filtering, channel selection and demodulation to be done digitally. Higher centre frequencies were also desired to reduce the complexity of the analog mixing stage.

Chapter 2 reviewed the operation of ΔΣ A/D conversion and compared LPΔΣ and BPΔΣ A/D converters. Switched-C technology was chosen over continuous-time methods for implementation because it was a proven technology for high resolution at baseband. Continuous-time is expected to dominate at very high speeds but, for the specifications outlined in Table 1.1, the switched-C approach was considered optimal. Single stage and two stage (MASH) topologies were compared for the implementation. MASH modulators were shown to produce stable high-order noise shaping, but required precision matching between analog and digital filters. For this reason a single stage topology was selected.

Chapter 3 explored architectures which were capable of producing high resolution A/D conversion with low oversampling ratios (OSR). It was shown that if a low OSR is
used the SNR will not increase significantly as the order of the modulator is increased. However, by slightly increasing the maximum gain of the NTF used in the modulator, large increases in in-band attenuation could be obtained, resulting in much larger SNRs. To take advantage of this trade-off, multi-level quantizers were required to reduce the noise power being fed back to the filter, otherwise the system would become unstable. Simulated results showed that by taking advantage of the added stability when going from a 2-level to a 3-level quantizer, in an 8th-order modulator, an increase in SNR of 18dB could be obtained. Linearity problems with the multi-level D/A converter were addressed by using randomizing approaches [24][25] to convert D/A errors into white noise. For low OSR systems, it was shown that a large portion of this white noise lies in-band, reducing the SNR to approximately 12 bits. However, if differential circuits are used in the implementation, it is conceivable that 3 levels could be obtained quite accurately with careful design and layout. Therefore, to meet the radio specifications a 3-level quantizer and an 8th-order NTF, which had a maximum gain of 5dB, could be used. Simulated results for the resulting modulator gave a SNR of 87dB.

Although digital error correction schemes were not discussed (since it was considered desirable to avoid making the decimation side any more complicated than need be) a simple procedure for correcting 3-levels to 20 bit accuracy has recently been reported[42] making the work presented here much more viable.

Chapter 4 contained the high-speed analog circuits required to meet the sampling frequency desired by industry. The circuits were designed in a 0.8μm BiCMOS process (±2.5V) and included a fully differential folded cascade OTA with continuous-time CMFB, a pseudo-ECL comparator, switches, a clock generator, a D/A converter, and a sample-and-hold. We attempted to meet all of the specifications set out in Table 1.1 except the power constraint. This was considered a little too stringent for the first BiCMOS run.

Chapter 5 focused on determining the maximum sampling speed obtainable from a switched-C BPAΣ modulator and what the limiting factors would be. Two different 2nd-
order structures were implemented to investigate this upper limit and were named the LDI modulator and FE modulator. The LDI modulator was chosen for its capability of delivering an infinite Q filter in spite of capacitor mismatches. The FE modulator was selected for the reduced OTA bandwidth required, even though the Q of the filter was dependent on capacitor matching. Experimental results showed that the FE modulator gave a speed advantage over the LDI modulator and the sensitivity of Q to capacitor errors did not appear to seriously degrade SNR. Higher order modulators are more tolerant to Q errors so the FE modulator would be well suited for the required 8th-order BPAΣ modulator.

Experimental results showed that the SNR of the LDI and FE modulators increased by 9dB/octave (as should be the case for 1st-order noise shaping) up to clock frequencies of 30MHz and 40MHz, respectively. After these points the effects of incomplete OTA settling started to effect modulator performance. The slow settling of the OTA was determined to be due to the large parasitic input capacitance of the folded cascode OTA and the low slew rate.

6.2 Future Work

To meet the radio specifications given in Table 1.1 the FE biquad would need to be cascaded 4 times. The resulting modulator (in single-ended form) is shown in Fig. 6.1.
To obtain the capacitor values for this system the NTF needs to be derived (eq. 6.1) and set equal to the desired NTF derived in (eq. 3.1). This would be difficult by hand but with software such as Mathematica [43] this is not a problem. The feed-in capacitor values could be determined by deriving the STF of the 8\textsuperscript{th}-order modulator in Fig. 6.1 (eq. 6.2) and setting it equal to the desired STF derived in (eq. 3.2).

\[
\text{NTF} = \frac{T_1T_2T_3T_4}{T_1T_2T_3T_4 - B_0I^3 - B_1I^4 - B_2I^5 - B_3I^6 - B_4I^7 - B_5I^8 - B_6I^9 - B_7I^{10} - B_8I^{11}}
\]  
(6.1)

where: \( I = z^{-1} \), \( T_n = I^2 - R_n + (R_n = D_n) \)

\[
\text{STF} = \frac{A_0I^3 + A_1I^4 + A_2I^5 + A_3I^6 + A_4I^7 + A_5I^8 + A_6I^9 + A_7I^{10} + A_8I^{11}}{T_1T_2T_3T_4 - B_0I^3 - B_1I^4 - B_2I^5 - B_3I^6 - B_4I^7 - B_5I^8 - B_6I^9 - B_7I^{10} - B_8I^{11}}
\]  
(6.2)

Since 3-level modulators have been implemented and 3-level digital correction schemes have been done [42], more interesting research would be to build a S-level 8\textsuperscript{th}-order BPΔΣ modulator which required 5-levels to obtain a good stability margin but could possibly operate with just 3-levels. This would allow the designer to have the inner levels of the D/A converter selectable. One could determine if the system works for a known digital correction scheme (3-levels) and then switch in the inner levels and the 5-level digital correction scheme could be tested. One such NTF was selected from Fig. 3.3 which had a maximum gain of 7dB. The coefficient form of the NTF, obtained from filterX, is given in (eq. 6.3). A STF was also obtained and is given in (eq. 6.4).

\[
\text{NTF} = \frac{Y(z)}{N(z)} = \frac{b_0 + b_2z^2 + b_4z^4 + b_6z^6 + b_8z^8}{d_0 + d_2z^2 + d_4z^4 + d_6z^6 + d_8z^8}
\]  
(from filterX)  
(6.3)

\[
\begin{align*}
\{ & b_0 = b_8 = 1, \\
& b_2 = b_6 = 3.99167, \\
& b_4 = 5.98336 \}
\end{align*}
\]

\[
\begin{align*}
& d_0 = 0.22441, \\
& d_2 = 1.14243, \\
& d_4 = 2.41419 \end{align*}
\]

\[
\text{STF} = \frac{Y(z)}{U(z)} = \frac{a_1 + a_3z^3 + a_5z^5 + a_7z^7}{d_0 + d_2z^2 + d_4z^4 + d_6z^6 + d_8z^8}
\]  
(from filterX)  
(6.4)

\[
\begin{align*}
& \{ & a_1 = -0.060804, \\
& & a_3 = 0.023266, \\
& & a_5 = 0.060804 \}
\end{align*}
\]
Eq. 6.3 and eq. 6.4 were set equal to eq. 6.1 and eq. 6.2 respectively to obtain the required capacitor values for the 5-level 8\textsuperscript{th}-order BP\Delta\Sigma modulator (Table 6.1).

### TABLE 6.1 Unscaled capacitor values for the 5-level 8\textsuperscript{th}-order BP\Delta\Sigma A/D modulator shown in Fig. 6.1.

<table>
<thead>
<tr>
<th>Ratio</th>
<th>Value</th>
<th>Ratio</th>
<th>Value</th>
<th>Ratio</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>B\textsubscript{0}</td>
<td>0.0</td>
<td>A\textsubscript{0}</td>
<td>-0.0376</td>
<td>R\textsubscript{1}</td>
<td>-1.9657</td>
</tr>
<tr>
<td>B\textsubscript{1}</td>
<td>0.0220</td>
<td>A\textsubscript{1}</td>
<td>-0.0181</td>
<td>R\textsubscript{2}</td>
<td>-2.0343</td>
</tr>
<tr>
<td>B\textsubscript{2}</td>
<td>0.1379</td>
<td>A\textsubscript{2}</td>
<td>-0.0564</td>
<td>R\textsubscript{3}</td>
<td>-1.9155</td>
</tr>
<tr>
<td>B\textsubscript{3}</td>
<td>0.1722</td>
<td>A\textsubscript{3}</td>
<td>-0.0185</td>
<td>R\textsubscript{4}</td>
<td>-2.0845</td>
</tr>
<tr>
<td>B\textsubscript{4}</td>
<td>0.7759</td>
<td>A\textsubscript{4}</td>
<td>-0.0134</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B\textsubscript{5}</td>
<td>0.4257</td>
<td>A\textsubscript{5}</td>
<td>0.0651</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B\textsubscript{6}</td>
<td>1.1442</td>
<td>A\textsubscript{6}</td>
<td>0.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B\textsubscript{7}</td>
<td>0.0</td>
<td>A\textsubscript{7}</td>
<td>0.06</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

All \( C_{r_n} = C_{d_n} \)

All \( C_{r_n} = C_{s_n} = 1 \)

n = 1, 2, 3, 4

All integrating caps. = 1

Example: \( B_0 = C_{40}/C_{10} \) or \( R_1 = C_{r1}/C_{d0} \)

To make sure no errors were made in determining these capacitor values, the 8\textsuperscript{th}-order BP\Delta\Sigma modulator was simulated in SWITCAP\textsuperscript{2}[44] using the capacitor values in Table 6.1. The quantizer in Fig. 6.1 was replaced by an addition stage such that an AC analysis could be performed in SWITCAP\textsuperscript{2} to obtain the NTF and STF. The results were compared to the ideal NTF and STF obtained from filtor\textsuperscript{X} in Fig. 6.2 and it can be seen that rounding the capacitor values off to 4 decimal places had little effect on the results. A 5-level quantizer should be used in SWITCAP\textsuperscript{2} and the maximum output of each integrator determined. The capacitors could then be scaled to maximize dynamic range of each integrator.

In the FE structure (Fig. 6.1) all the OTAs get sampled on phase 2. Since this is the phase that the OTA will require most time to slew (load capacitance is connected) it might be a good idea to increase the length of phase 2 (for example to give a 60/40 duty cycle).
An improved OTA will be required to meet the 80MHz sampling frequency outlined by the digital radio market. One such OTA that will meet speed requirements is the telescopic cascode OTA (Fig. 6.3). By using NMOS devices for the input, this OTA can obtain the same $g_m$ as the folded cascode OTA with devices that are $1/3$ the size. This will decrease parasitic input capacitance resulting in a faster closed loop time constant. Also, by using the emitter followers as current buffers to drive the load capacitances, a larger slew rate can be obtained ($SR \approx \frac{I_{bias}}{C_c}$ but $C_c \ll C_L$). To prevent large overshoots in the

### TABLE B.2 Simulated results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain</td>
<td>57dB</td>
</tr>
<tr>
<td>$f_t$</td>
<td>630MHz</td>
</tr>
<tr>
<td>PM</td>
<td>64°</td>
</tr>
<tr>
<td>*Settling time</td>
<td>5.2ns</td>
</tr>
<tr>
<td>Slew-rate</td>
<td>1400V/µs</td>
</tr>
<tr>
<td>output range</td>
<td>4.6V</td>
</tr>
<tr>
<td>Power</td>
<td>25mW</td>
</tr>
</tbody>
</table>

* $C_c \approx 0.6pF$, settle to 0.1%
output waveform, the voltage at the emitter of Q1 and Q2 has to be able to change faster than the voltage at the base of Q1 and Q2. This requires large currents to be used in the emitter followers resulting in large power dissipation.

For hand held applications a reduction in the power dissipation is desired. To meet the power requirements outlined in Table 1.1 and to prevent slew rate limitations a different form of amplification will be required. A suggestion would be to look into class AB amplifiers [33] or inverter type amplifiers [45]. The standard single stage amplifiers will not be able to meet the slew rate and power requirements simultaneously unless a method of dynamically biasing the tail current is developed [46]. An important note in designing OTAs for BPΔΣ modulators, rather than LPΔΣ modulators, is that the integrators used will require a gain greater than one. This results in increasing the integrator time constant which can result in long settling times. Therefore, the OTA should be checked in a transient analysis with the actual scaled capacitor values to make sure $5\tau$ settling is obtained in the allowed time.

Another interesting project would be to design an AM/PM radio using the present 2nd-order BPΔΣ modulator. A/D conversion could be performed on AM RF or PM IF. This would be an interesting project allowing the designer to build some analog front-end circuits as well as some very complicated digital circuits.
APPENDIX A

Effects of Non-ideal OTAs on Switched-C Biquads

Filters used in ΔΣ modulators require that there poles be placed very accurately since these poles will determine the band of frequencies that quantization noise will be filtered away from. Errors in the phase of the filter pole results in shifting the centre frequency of the modulator from ideal, reducing SNR in the band selected for decimation. Magnitude errors results in lowering the Q of the filter again reducing the SNR. Low Q also produces “deadband” behavior and may result in intermodulation distortion[9]. The effects of finite gain and bandwidth on switch-C biquads for zero output impedance op-amps were previously investigated by Martin and Sedra [32]. These results were then generalized to transconductance op-amps, where the transient due to charging amplifier loads is important, by Ribner and Copeland [41]. Neither of these methods considered slew rate limited op-amps or input and output parasitic capacitances. These extensions are made in this appendix.

The first part of this appendix determines the effect of non-ideal OTAs on the transfer function of the $1/2$-delay and 1-delay non-inverting integrators. These results are then used to determine the pole location of the lossless discrete integrator (LDI) filter and “Forward Euler” (FE) filter and hence the magnitude and phase errors that can be expected with each.

A.1 $1/2$-Delay Non-inverting Integrator

The $1/2$-delay non-inverting integrator is shown in Fig. A. 1. Two switch capacitor inputs are shown: $C_1$ the feed-in capacitor of interest and $C_4$ representing all other capacitor feed-ins. To derive the transfer function $V_o(z)/V_i(z)$ superposition is used, meaning
all other input sources are grounded except \( V_1 \). During \( \theta_1 \) the input capacitor \( C_1 \) is connected to \( V_1 \), capacitor \( C_4 \) is shorted to ground and the output capacitor \( C_3 \) is connected to the next stage (virtual ground of an OTA). On \( \theta_2 \) the OTA removes the charge from the input capacitors and stores it across \( C_2 \) as well as charging up the output capacitor \( C_3 \). Due to non-ideal OTAs, all the charge is not removed from the input capacitors on \( \theta_2 \) and magnitude and phase errors result.

During \( \theta_1 \) the input capacitor \( C_1 \) is connected to \( V_1 \), capacitor \( C_4 \) is shorted to ground and the output capacitor \( C_3 \) is connected to the next stage (virtual ground of an OTA). On \( \theta_2 \) the OTA removes the charge from the input capacitors and stores it across \( C_2 \) as well as charging up the output capacitor \( C_3 \). Due to non-ideal OTAs, all the charge is not removed from the input capacitors on \( \theta_2 \) and magnitude and phase errors result.

![Figure A.1](image)

**Figure A.1**

- **a)** 1/2-delay non-inverting integrator
- **b)** clock phasing diagram
- **c)** charging diagram when \( \theta_1 \) is “high”
- **d)** charging diagram when \( \theta_2 \) is “high”

### A.1.1 OTAs with Finite DC Gain

In this section the transfer function of the 1/2-delay non-inverting integrator is derived assuming the OTAs have finite DC gain but infinite bandwidth and unlimited slew rate. The output voltage \( V_o(n) \) (node [B] in Fig. A. 1) at the end of \( \theta_2 \) is given by eq. A.1.

\[
V_o(n) = -V_2(n) - \frac{1}{A_o} V_o(n)
\]  
(A.1)
\( V_2(n) \) is derived using the conservation of charge law at node [A] in Fig. A.1.

\[
\Delta q_{C_2} + \Delta q_{C_i} + \Delta q_{C_p} + \Delta q_{C_4} = 0 
\]

where: \( \Delta q = C A V \)

Substitute the change in voltage from time \((n-1) \rightarrow n\) into eq.A.2 to get eq.A.3.

\[
C_2(V_2(n-1) - V_2(n)) + C_1 \left(-V_i(n-1/2) - \frac{-Vo(n)}{A_0}\right) + C_p \left(\frac{-Vo(n-1)}{A_0} - \frac{-Vo(n)}{A_0}\right) + C_4 \left(0 - \frac{-Vo(n)}{A_0}\right) = 0
\]

Simplifying eq.A.3 and using the z-transform, an expression for \( V_z \) is derived:

\[
V_2(z)(1-z^{-1}) = -\frac{C_1}{C_2} z^{-1/2} V_z(z) + \frac{1}{A_0} \left(\frac{C_1 + C_4 + C_p}{C_2} - \frac{C_p}{C_2} z^{-1}\right) V_0(z)
\]

Substitute eq.A.4 into the z-transform of eq.A.1 and simplify to obtain the transfer function of the 1/2-delay non-inverting integrator which uses finite gain OTAs.

\[
\frac{V_0(z)}{V_i(z)} = \frac{C_1/C_2 \left(1 + \left(\frac{C_1 + C_2 + C_4 + C_p}{A_0}/C_2\right)\right)z^{1/2}}{z-1 - \left(\frac{C_1 + C_2 + C_4 + C_p}{A_0}/C_2\right)}
\]

Making the observation:

\[
1/\left(1 + \left(\frac{C_1 + C_2 + C_4 + C_p}{A_0}/C_2\right)\right) = 1 - \frac{(C_1 + C_2 + C_4 + C_p)/C_2}{A_0}
\]

eq.A.5 simplifies to eq.A.7.

\[
\frac{V_0(z)}{V_i(z)} = \frac{C_1/C_2 \left(1 - \left(\frac{C_1 + C_2 + C_4 + C_p}{A_0}/C_2\right)\right)z^{1/2}}{z - \left(1 - \left(\frac{C_1 + C_4}{A_0}/C_2\right)\right)} = \frac{C_1/C_2 p z^{1/2}}{z - M}
\]

A.1.2 OTAs with Finite Bandwidth and Slew Rate Limitations

In this section the transfer function of the 1/2-delay non-inverting integrator will be derived assuming the OTAs have infinite DC gain but finite bandwidth and limited slew
rate. To simplify this procedure the transconductance amplifier is assumed to have a single pole “roll-off”:

$$A(s) = \frac{\omega_1}{s}$$  \hspace{1cm} (A.8)

Typical waveforms that are observed at the input and output of the OTA from a transient analysis are shown in Fig. A.2.

At the instant \( \theta_2 \) goes “high” transients occur at the input and output of the transconductance amplifier due to charge redistributions. The initial voltages at the input and output of the OTA due to this charge redistribution will be referred to as \( V_i(n-1/2)^+ \) and \( V_o(n-1/2)^+ \) respectively. The value of these voltages are derived by using charge conservation at node [A] and [B] in Fig. A.1 for the time interval \( (n-1/2) \rightarrow (n-1/2)^+ \). Assume that the switches are much faster than the OTA.

From node [B]:

$$V_o(n - 1/2)^+ = \frac{C_2 + C_{lp}}{C_2 + C_{lp} + C_3} V_o(n - 1/2) + \frac{C_2}{C_2 + C_{lp} + C_3} V_i(n - 1/2)^+$$  \hspace{1cm} (A.9)
From node [A]:

$$V_1(n-1/2)^+ = -\frac{C_1}{C_w}V_i(n-1/2) - \frac{C_2C_3}{C_w(C_2+C_{ip}+C_3)}V_o(n-1/2) \quad (A.10)$$

where: \( C_w = C_1 + C_4 + C_p + \frac{C_2(C_{ip}+C_3)}{C_2+C_{ip}+C_3} \)

After the initial charge transfer, during the time interval \((n-1)^+ \rightarrow n\), the output voltage of the OTA will slew for a portion of the time and then settle linearly (eq. A.11).

$$\frac{d}{dt}V_o(t) = \begin{cases} -\frac{SR}{\omega V_1(t)} & t \leq t_{slew} \\ -\omega V_1(t) & t > t_{slew} \end{cases} \quad (A.11)$$

where: \( t_{slew} \) is the amount of time the OTA spends slewing

The output voltage of the OTA can be related to the input of the OTA by using KCL at node [A]:

$$C_2\frac{d}{dt}V_2(t) + (C_1 + C_4 + C_p)\frac{d}{dt}V_1(t) = 0 \quad (A.12)$$

But \( V_2(t) = V_1(t) - V_o(t) \) so eq. A.12 becomes:

$$\frac{d}{dt}V_o(t) = \left( \frac{C_1 + C_4 + C_p + C_2}{C_2} \right) \frac{d}{dt}V_1(t) \quad (A.13)$$

Substituting eq. A.13 into eq. A.11 and using Laplace transforms, an expression for \( V_1(t) \) is obtained:

$$V_1(t) = \begin{cases} V_1(n-1/2)^+ - \beta (SR) t & t \leq t_{slew} \\ V_1(t_o)e^{-\frac{1}{\tau}(t-t_{slew}-t_{overlap})} & t > t_{slew} \end{cases} \quad (A.14)$$

where: \( \beta = \frac{C_2}{(C_1 + C_4 + C_p + C_2)} \) (feedback factor)

\( 2 = 1/\beta \omega_1 \) (the integrator rime constant)

\( t_{overlap} \) is the time between non-overlapping clock phases.

Assuming that \( t > t_{slew} \) a one line expression for \( V_1(t) \) can be obtained:

$$V_1(t) = (V_1(n-1/2)^+ - \beta (SR) t_{slew}) e^{-\frac{1}{\tau}(t-t_{slew}-t_{overlap})} \quad (A.15)$$
The amount of time the OTA spends slewing is determined by substituting 
\[ V_1(t_{\text{slew}}) = \frac{SR}{\omega_l} \] (from eq.A.11) into \[ V_1(t_{\text{slew}}) = V_1(n - 1/2)^+ - \beta (SR)t_{\text{slew}} \] (from eq.A.14):

\[ t_{\text{slew}} = \frac{V_1(n - 1/2)^+}{\beta (SR)} - \tau \]  \hspace{1cm} (A.16)

An expression for \( V_1(n) \) can be obtained by substituting eq.A.16 into eq.A.15 and solving at time \( n \):

\[ V_1(n) = \left(\frac{SR}{\omega_l}\right) e^{-\frac{1}{\tau} \left( \frac{1}{2f_s} - \frac{V_1(n - 1/2)^+}{\beta (SR)} + \tau - t_{\text{overlap}} \right)} \]  \hspace{1cm} (A.17)

The result shows that \( V_1(n) \) is a non-linear function of \( V_1(n - 1/2)^+ \) which greatly increases the complexity of the problem. To simplify eq.A.17 the worst case condition will be considered. The worst condition occurs when the output of the OTA must swing its maximum range \( (V_1(n - 1/2)^+/\beta = V_{\text{max}}) \) this would result in maximum slewing time be subtracted away from the time allowed for linear settling, for all input. Therefore to reduce the error in this approximation a linear correction factor was placed in front of the exponential \( (V_1(n - 1/2)^+/\beta V_{\text{max}}) \) such that for smaller inputs, for which the OTA might not slew but the approximation still subtracts maximum slew time, the error in \( V_1(n) \) would be reduced. Therefore, a linear approximation to eq.A.17 is:

\[ V_1(n) = \frac{SR}{\omega_l} \left( \frac{V_1(n - 1/2)^+}{\beta V_{\text{max}}} \right) e^{-\frac{1}{\tau} \left( \frac{1}{2f_s} - \frac{V_{\text{max}}}{SR} + \tau - t_{\text{overlap}} \right)} = \zeta V_1(n - 1/2)^+ e^{-k} \] \hspace{1cm} (A.18)

where: \[ k = \frac{1}{\tau} \left( \frac{1}{2f_s} - \frac{V_{\text{max}}}{SR} + \tau - t_{\text{overlap}} \right) \]

\[ \zeta = (\tau SR)/V_{\text{max}} \]

To relate this to the output eq.A.13 is simplified and solved at \( t = n \) to give:

\[ V_o(n) - V_o(n - 1/2)^+ = (1/\beta) (V_1(n) - V_1(n - 1/2)^+) \] \hspace{1cm} (A.19)

Substituting eq.A.18 into eq.A. 19 an expression for \( V_o(n) \) is obtained:
V_o(n) = V_o(n - 1/2) + \frac{1}{1/\beta} (1 - \zeta e^{-k}) V_1(n - 1/2) \tag{A.20}

Substitute eq.A.9 and eq.A.10 into eq.A.20 to obtain:

V_o(n) = V_o(n - 1/2) \left( 1 - \frac{C_3 (C_2/\beta)}{C_w(C_2 + C_{lp} + C_3)} \zeta e^{-k} \right) + \frac{C_1}{C_2} V_1(n - 1/2) \left( 1 - \frac{C_2}{\beta C_w} \zeta e^{-k} \right) \tag{A.21}

V_o(n - 1/2) = V_o(n - 1) - (1 - e^{-\kappa_1}) V_1(n - 1) \tag{A.22}

where: \( \kappa_1 \) is the exponential constant associated with the integrator on \( \theta_1 \).

During \( \theta_1 \) both input and output capacitors are disconnected therefore \( \kappa_1 \) is quite large and \( V_o(n - 1/2) \) becomes:

V_o(n - 1/2) = V_o(n - 1) - V_1(n - 1) \tag{A.23}

Substituting eq.A.23 into eq.A.21 and taking the z-transform we arrive at the transfer function for the 1/2-delay non-inverting integrator which uses OTAs with finite bandwidth and slew rate limitations.

\[
\frac{V_o(z)}{V_1(z)} = \frac{\frac{C_1}{C_2} (1 - \alpha \zeta e^{-k}) z^{1/2} + \frac{C_1}{C_w} \zeta e^{-k}}{z - (1 - \lambda \zeta e^{-k})} \tag{A.24}
\]

Taking into consideration that \( \frac{C_1}{C_w} \zeta e^{-k} \approx 0 \) eq.A.24 simplifies into eq.A.25.

\[
\frac{V_o(z)}{V_1(z)} = \frac{\frac{C_1}{C_2} (1 - \alpha \zeta e^{-k}) z^{1/2}}{z - (1 - \Lambda \zeta e^{-k})} = \frac{C_1 p z^{1/2}}{z - \Lambda} \tag{A.25}
\]

where: \( \alpha = C_2' / (\beta C_w) \), \( \beta = C_2' / (C_1 + C_4 + C_p + C_2) \), \( \zeta = (\tau SR)/V_{max} \)

\[
\Lambda = \frac{C_3 (C_2/\beta)}{C_w(C_2 + C_{lp} + C_3)} \), \( k = \frac{1}{\tau} (\frac{1}{2f_s} - \frac{V_{max}}{SR} + \tau - \tau_{overlap}) \)

\[
C_w = C_1 + C_4 + C_p + \frac{C_2 (C_{lp} + C_3)}{C_2 + C_{lp} + C_3}, \tau = 1 / (\beta \omega)
\]

A.2 1-Delay Non-inverting Integrator

The 1-delay non-inverting integrator (Fig. A.3) differs from the 1/2-delay non-inverting integrator by having its input and output capacitors connected to the OTA on
opposite clock phases. As a result the integrator has less total loop capacitance on the individual clock phases and faster integrator time constants are possible. However, the OTA now has to settle two transients; one on $\theta_1$ when the input capacitor is connected to the virtual ground of the OTA and another on $\theta_2$ when the load capacitor, which was just discharged, is connected to the output.

**A.2.1 OTAs with Finite DC Gain**

The response of the l-delay non-inverting integrator which uses OTAs that have infinite bandwidth, unlimited slew rate but finite DC gain can be shown to be the same as those for the $1/2$-delay non-inverting integrator except now the output is one full phase behind the input.
A.2.2 OTAs with Finite Bandwidth and Slew Rate Limitations

The effects of finite bandwidth and slew rate limited OTAs on the performance of the 1-delay non-inverting integrator are determined by splitting up the analysis into two parts \((n - 1) \rightarrow (n - 1/2)\) and \((n - 1/2) \rightarrow n\).

\[
\frac{V_o(z)}{V_i(z)} = \frac{C_1 (1 - \frac{(C_1 + C_2 + C_4 + C_p) / A_0}{z - \left(1 - \frac{(C_1 + C_4) / A_0}{C_2}\right)}} = \frac{C_1 p}{Z - M} \tag{A.26}
\]

**Figure A.4** The transient response at the input \((V_i)\) and output \((V_o)\) of the 1-delay non-inverting integrator. Figure intended to illustrate initial charge redistribution, OTA slewing and linear settling.

**Timeinterval** \((n - 1) \rightarrow (n - 1/2)\):

To derive \(V_o(n - 1/2)\) the integrator is analyzed when \(\theta_1\) is “high”. This is almost identical to the analysis performed on the 1/2-delay non-inverting case and an expression for \(V_o(n - 1/2)\) can be written directly. The subscript “1” is attached to many of the constants to distinguish between phases, since these constants will be different for each phase.
\[ V_o(n - 1/2) = V_o(n - 1)^+ - (1/\beta_1)\left(1 - \xi_1 e^{-k_1}\right)V_1(n - 1)^+ \]  
(A.27)

where: \( \beta_1 = C_2 / (C_1 + C_4 + C_p + C_2) \), \( \xi_1 = \tau_1 (SR)_1 / V_{\text{max}} \)

\[ k_1 = \frac{1}{\tau_1} \left( \frac{1}{2f_s} - \frac{V_{\text{max}}}{(SR)_1} + \tau_1 - t_{\text{overlap}} \right) \]

\( V_o(n - 1)^+ \) and \( V_1(n - 1)^+ \) are derived by using charge conservation at node [B] and node [A], respectively, at the instant \( \theta_1 \) goes high in Fig. A.3. (assumption: \( V_1(n - 1) = 0 \)).

\[ V_o(n - 1)^+ = V_o(n - 1) + \frac{C_2}{C_2 + C_{ip}}V_1(n - 1)^+ \]  
(A.28)

\[ V_1(n - 1)^+ = -\frac{C_1(C_2 + C_{ip})}{(C_1 + C_4 + C_p)(C_2 + C_{ip}) + C_2C_{ip}}V_1(n - 1) \]  
(A.29)

Substituting eq.A.29 and eq.A.28 into eq.A.27 \( V_o(n - 1/2) \) is obtained:

\[ V_o(n - 1/2) = V_o(n - 1) + \frac{C_1}{C_2}\left(1 - \frac{(C_2/\beta_1)\xi_1 e^{-k_1}}{C_1 + C_4 + C_p + C_2C_{ip}/(C_2 + C_{ip})}\right)V_1(n - 1) \]  
(A.30)

**Time interval** \( (n - 1/2) \rightarrow n: \)

To derive \( V_o(n) \) the integrator is analyzed when \( \theta_2 \) is “high”. At the instant \( \theta_2 \) goes high the load capacitor \( C_3 \), which was just discharged, is connected to the OTA pulling the output towards the common-mode output voltage. The voltages at the input and output of the OTA at this instant are derived using the conservation of charge law at node [A] and [B] in Fig. A.3:

\[ V_o(n - 1/2)^+ = \frac{C_2 + C_p}{C_2}V_1(n - 1/2)^+ + V_o(n - 1/2) \]  
(A.31)

\[ V_1(n - 1/2)^+ = \frac{C_2 + C_3 + C_{ip}}{C_2}V_o(n - 1/2)^+ - \frac{C_2 + C_{ip}}{C_2}V_o(n - 1/2) \]  
(A.32)

The same type of analysis that was used to derive \( V_1(n) \) and \( V_o(n) \) for the **1/2-delay non-inverting integrator** can be used here to obtain eq.A.33 and eq.A.34. The subscript “2” refers to the operating phase.
\[ V_{\nu}(n) = \zeta_2 V_1(n-1) e^{-k_2} \]  
\( (A.33) \)

where:  
\[ k_2 = \frac{1}{\tau_2} \left( \frac{1}{2f_s} - \frac{V_{\text{max}}}{(\text{SR})_2} + \tau_2 - \tau_{\text{overlap}} \right) \]
\[ \tau_2 = \frac{1}{\beta_2 \omega_{t2}}, \beta_2 = C_2 / (C_2 + C_p), \zeta_2 = (\text{SR})_2 \tau_2 / V_{\text{max}} \]

\[ V_0(n) = V_0(n-1/2)^+ - \left( \frac{1}{\beta} \right) (1 - \zeta_2 e^{-k_2}) V_1(n-1/2)^+ \]  
\( (A.34) \)

Substituting eq.A.31 and eq.A.32 into eq.A.34 an expression for \( V_0(n) \) as a function of \( V_0(n-1/2) \) is obtained:

\[ V_0(n) = \left( 1 - \frac{C_3 \zeta_2 e^{-k_2}}{C_3 + C_{lp} + C_2 C_p / (C_2 + C_p)} \right) V_0(n-1/2) \]  
\( (A.35) \)

Substituting eq.A.30 into eq.A.35 and taking the z-transform we arrive at the transfer function for the 1-delay non-inverting integrator which uses OTAs with finite bandwidth and slew rate limitations.

\[ \frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2} \frac{(1 - \alpha \zeta_1 e^{-k_1}) (1 - \lambda \zeta_2 e^{-k_2})}{z - (1 - \lambda \zeta_2 e^{-k_2})} \frac{(C_1 / C_2) E}{Z-F} \]  
\( (A.36) \)

where:  
\[ \alpha = \frac{C_1 + C_4 + C_p + C_2}{C_1 + C_4 + C_p + C_2 C_{lp} / (C_2 + C_{lp})} \]
\[ \lambda = \frac{C_3}{C_3 + C_{lp} + C_2 C_p / (C_2 + C_p)} \]

### A.3 Errors expected with the LDI Biquad

The LDI filter consists of two 1/2-delay integrators (Fig. 5.2). The location of the filter poles can be determined by calculating the gain around the loop consisting of capacitors \( C_r, C_{i1}, C_x \) and \( C_{i2} \) and solving eq.A.37.

\[ 1 - \text{LoopGain} = 0 \]  
\( (A.37) \)

The general form for the transfer function of the 1/2-delay non-inverting integrator which used non-ideal amplifiers was calculated in section A.1 and is repeated below.
Use eq.A.38 to derive the loop gain of the filter and substitute it into eq.A.37.

$$1 + \frac{c_r}{C_{i1}} \frac{P_1 z^{1/2}}{z - M_1} \frac{C_x}{C_{i2}} \frac{P_2 z^{1/2}}{z - M_2} = 0$$

(A.39)

Simplify this equation to get:

$$z^2 - \left( M_1 + M_2 - \frac{C_r}{C_{i1}} C_x \frac{P_1}{C_{i2}} P_2 \right) z + M_1 M_2 = 0$$

(A.40)

From eq.A.40 the magnitude of the filter pole is derived:

$$|z| = \sqrt{M_1 M_2}$$

(A.41)

and its angular frequency:

$$\angle z = \tan^{-1} \left( \frac{M_1 M_2 - \left( M_1 + M_2 - \frac{C_r}{C_{i1}} C_x \frac{P_1}{C_{i2}} P_2 \right)^2}{ M_1 M_2 - \left( M_1 + M_2 - \frac{C_r}{C_{i1}} C_x \frac{P_1}{C_{i2}} P_2 \right)^2 / 2} \right) / 4$$

(A.42)

In our design the notch frequency was selected to be at $f_s/4$. Therefore, the error in the filter poles angular frequency ($\Delta \theta$) is approximately:

$$\Delta \theta = \left( M_1 + M_2 - \frac{C_r}{C_{i1}} C_x \frac{P_1}{C_{i2}} P_2 \right) / 2$$

(A.43)

Relating this to the centre frequency $f_o$:

$$\frac{\Delta f_o}{f_o} = \frac{f_s}{2\pi f_o} \Delta \theta$$

(A.44)

The resulting magnitude and phase errors in the filter pole due to the use non-ideal OTAs in the LDI structure are summarized in Table A.1.
### TABLE A.1 Effects of non-ideal OTAs on the LDI Biquad

<table>
<thead>
<tr>
<th>Error Type</th>
<th>Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Errors due to finite DC gain</td>
<td>( \Delta \theta = \left( \frac{(M_1 + M_2 - RP_1 P_2)}{2} \right) \left( \frac{1}{\sqrt{M_1 M_2} - (M_1 + M_2 - RP_1 P_2)^2/4} \right) )</td>
</tr>
<tr>
<td>Errors due to finite BW and SR use the adjacent M_n, P_n, R</td>
<td>( M_n = 1 - \frac{C_{\text{in}, n}}{C_{\text{in}, n} A_0}, \quad P_n = M_n - \frac{C_{\text{in}, n} + C_p}{C_{\text{in}, n} A_o}, \quad R = \frac{C_r C_i}{C_{\text{i1}} C_{\text{i2}}} )</td>
</tr>
</tbody>
</table>

**Subscript Notes:**
- \( n \) ... \( n^{th} \) integrator (either 1 or 2)
- \( C_{\text{a,n}}, \ldots \) all switch capacitors connected to the input of OTA \( n \)
- \( C_{\text{o,n}}, \ldots \) all switch capacitors connected to the output of OTA \( n \)
- \( C_l, \ldots \) integrator capacitor of OTA \( n \)
- \( C_p, \ldots \) parasitic capacitance at the input of the OTA
- \( C_{ip}, \ldots \) parasitic capacitance at the output of the OTA
- \( \xi_n = (\tau_n SR_n)/2 \ldots \) linear adjustment for slewing condition
- \( \tau_n = (C_{\text{a,n}} + C_p + C_{ip})/(C_{\text{i,n}} \omega_n) \ldots \) integrator time constant
- \( \omega_n = g_m/C_{\text{i,n}}, \ldots \) unity gain frequency of OTA
- \( K_n = (1/\tau_n) \left( \frac{1}{2f_s} + \frac{2}{SR_n} + \tau_n - t_{ol} \right) \ldots \) exponential constant
- \( t_{ol} \ldots \) time used up by non-overlapping clock

### A.4 Errors expected with the FE Biquad

The “Forward Euler” (FE) biquad is made up of two 1-delay non-inverting integrators (Forward Euler integrators). The general form of the transfer function for the 1-delay non-inverting integrator which used non-ideal amplifiers was derived in section A.2 and is repeated here.
With the FE structure there are two loops which determine the poles location; one consists of capacitors \( C_r, C_{i1}, C_x \) and \( C_i \) and the other consists of capacitors \( C_d \) and \( C_{i2} \). Poles for this filter are given by solutions to eq. A.46.

\[
1 + \frac{C_r}{C_{i1} C_{i2}} \frac{E_1 E_2}{(z - F_1)(z - F_2)} + \frac{C_d}{C_{i2}} \frac{E_2}{(z - F_2)} = 0
\]  
(A.46)

Simplified:

\[
z^2 - \left(F_1 + F_2 - \frac{C_d}{C_{i2}} E_2\right)z + F_1 F_2 + \frac{C_r}{C_{i1}} \frac{C_x}{C_{i2}} (E_1 E_2) - \frac{C_d}{C_{i2}} E_2 F_1 = 0
\]  
(A.47)

The magnitude of the filter pole is given by eq. A.48 and its angular frequency by eq. A.49.

\[
|z| = \sqrt{\frac{F_1 F_2 + \frac{C_r}{C_{i1}} \frac{C_x}{C_{i2}} (E_1 E_2) - \frac{C_d}{C_{i2}} E_2 F_1}{\left|F_1 + F_2 - \frac{C_d}{C_{i2}} E_2\right|^2 / 4}}
\]  
(A.48)

\[
\angle z = \text{atan} \left( \frac{|z|^2 - \left(F_1 + F_2 - \frac{C_d}{C_{i2}} E_2\right)^2 / 4}{\left(F_1 + F_2 - \frac{C_d}{C_{i2}} E_2\right) / 2} \right)
\]  
(A.49)

The error in the angular frequency is then

\[
\Delta \theta = \left(F_1 + F_2 - \frac{C_d}{C_{i2}} E_2\right) / 2
\]  
(A.50)

and relating this to \( f_o \) gives:

\[
\frac{\Delta f_o}{f_o} = \frac{f_s}{2 \pi f_o} \Delta \theta
\]  
(A.51)

The magnitude and phase errors that can be expected with the FE biquad due to non-ideal OTAs are summarized in Table A.2.
### TABLE A.2  Effects of non-ideal OTAs on the FE biquad

\[ i \mathcal{I} = \frac{F_1 F_2}{2} + \frac{1}{F_1 + F_2 - R E_2} \]

\[ \Delta \theta = \frac{1}{2} \left( \frac{(F_1 + F_2 - R E_2)^2}{(F_1 + F_2 - R E_2)^2} \right) \]

<table>
<thead>
<tr>
<th>Errors due to finite dc gain use the adjacent ( M_{n,m}, P_{n}, D &amp; R )</th>
<th>( F_n = 1 - \frac{C_{i_{n,m}}}{C_{i_{n,m}} A_0}, \quad E_n = F_n - \frac{C_{i_{n,m}} + C_p}{C_{i_{n,m}} A_0}, \quad R = \frac{C_{f} C_x}{C_{11} C_{12}}, \quad D = \frac{C_d}{C_{12}} )</th>
</tr>
</thead>
</table>

| Errors due to finite BW and SR use the adjacent \( M_{n,m}, P_{n} \) D \& R from previous row | \( F_n = 1 - \lambda_n \zeta_{n,m} e^{-K_{n,m}} \) \[ E_n = (1 - \alpha_n \zeta_{n,m} e^{-K_{n,m}}) (1 - \lambda_n \zeta_{n,m} e^{-K_{n,m}}) \] \[ \lambda_n = \frac{C_{o_{n,m}}}{C_{o_{n,m}} + C_p + C_{i_{n,m}} C_p / (C_{i_{n,m}} + C_p)} \] \[ \alpha_n = \frac{C_{i_{n,m}} + C_p + C_{i_{n,m}} C_p / (C_{i_{n,m}} + C_p)}{C_{i_{n,m}}} \] |

**Subscripts** \( n,m \ldots n^{th} \) integrator on the \( m^{th} \) clock phase

- \( C_{o_{n,m}} \ldots \) all switch capacitors connected to the input of \( OTA_n \)
- \( C_{o_{n,m}} \ldots \) all switch capacitors connected to the output of \( OTA_n \)
- \( C_{i_{n,m}} \ldots \) integrator capacitor of \( OTA_n \)
- \( C \ldots \) parasitic capacitance at the input of the OTA
- \( C_{ip} \ldots \) parasitic capacitance at the output of the OTA
- \( \zeta_{n,m} = \left( \frac{\tau_{n,m} SR_{n,m}}{2} \right) \ldots \) linear adjustment for slewing condition
- \( SR_{n,m} = \frac{I_{SR}}{C_{L,(n,m)}} \ldots \) slew rate
- \( \tau_{n,m} = \left( \frac{C_{o_{n,m}} + C_p + C_2}{C_2 \omega_{1(n,m)}} \right) \ldots \) integrator time constant
- \( \omega_{1(n,m)} = g_m / C_{L,(n,m)} \ldots \) unity gain frequency of OTA
- \( K_{n,m} = \left( \frac{1}{\tau_{n,m}} \right) \left( \frac{1}{2f_s} - \frac{2}{SR_{n,m}} + \tau_{n,m} - \tau_{o}\right) \) \ldots exponential constant
- \( \tau_{o} \ldots \) time used up by non-overlapping clock
References


